Lecture 17, Nov 15, 2023

More Design Examples

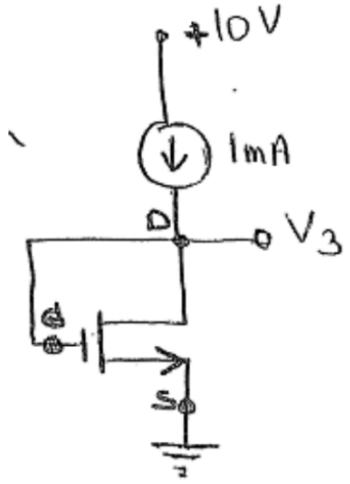

Figure 1: Design example 3.

- Example: feedback biasing: for the MOSFET circuit above, find the drain and source voltage and select a resistor to replace the current source
  - $V_S = 0$
  - $I_D = I_S = 2\,\text{mA}$ still because we assume a gate current of 0 at DC
  - $V_{GD} = 0$ forces us to be in saturation, since $V_{GD} < V_T$
  - $I_D = \frac{1}{2}k_n' \frac{W}{L}(V_{GS} - V_T)^2$, so we can solve for V_{GS} and pick the one that gives us saturation: $V_{GS} = 3.414\,\text{V}$
  - $V_G = V_S + V_{GS} = V_D$ to solve for V_{GS}
  - With V_{DD} and V_D and the current going through, we can find $1\,\text{mA} = \frac{V_D D - V_D}{R_D} \implies R_D = 6.59\,\text{k}\Omega$
  - By itself, this circuit doesn't do much, but we can use it to provide a stable reference current, as a building block in a current source circuit

PMOS Circuits

PMOS Transistor Equations

	Cutoff Mode	Triode Mode	Saturation Mode
Required Condition	$V_{GS} > V_t$	$V_{DS} \geq V_{GS} - V_t$ Or $V_{GD} \leq V_t$	$V_{DS} \leq V_{GS} - V_t$ Or $V_{GD} \geq V_t$
Determined Condition	$I_D = 0$	$I_D = k_p' \left(\frac{W}{L}\right)\left[(V_{GS} - V_t)V_{DS} - \frac{1}{2}V_{DS}^2\right]$	$I_D = \frac{1}{2}k_p' \left(\frac{W}{L}\right)(V_{GS} - V_t)^2$

Figure 2: PMOS transistor equations.

- For a PMOS, we have to flip the equations as above
- Positive current is defined as source to drain
- Note that V_T is negative for a PMOS, but otherwise has the same magnitude
- Given $V_T = -2\,\text{V}$, find V_D, V_S, determine an equivalent source resistor; assume $k_p' = 1\,\text{mA/V}^2$

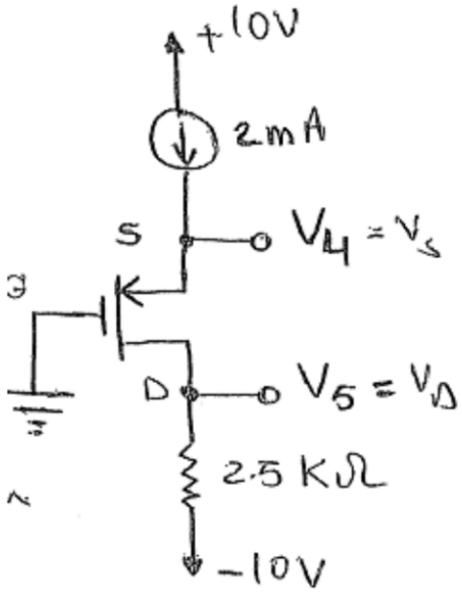

Figure 3: PMOS design example.

- We know $I_S = I_D = 2\,\text{mA}$, which already gives us $V_D = V_{SS} + R_D I_D = -5\,\text{V}$
  - Note the "negative supply" is still called V_{SS} even though it's now connected to the drain
- $V_{GD} = V_G - V_D = 5\,\text{V} > -2\,\text{V} = V_T$, so we have saturation mode
- $I_D = \frac{1}{2} k_p' \frac{W}{L} (V_{GS} - V_T)^2$ to get $V_{GS} = -4\,\text{V}$ as the voltage that avoids cutoff
- $V_S = V_G - V_S = 4\,\text{V}$
- Sanity check: we should normally have $V_S > V_D$ (typically the terminals will be laid out such that the higher voltages are higher on the page)
  - Due to saturation mode, we expect V_S to be quite a bit larger, which is the case
- This gives $R_S = 3\,\text{k}\Omega$