Lecture 1, Sep 8, 2023

The Need for Frequency Domain Analysis

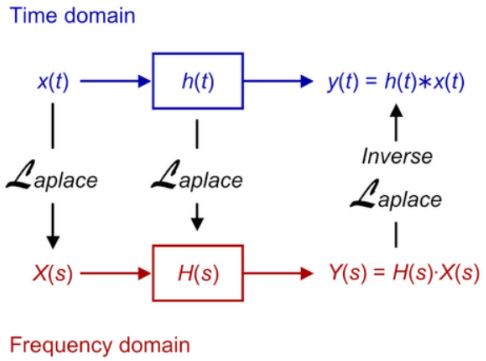

Figure 1: Summary of frequency domain analysis.

- Frequency domain analysis techniques allows us to more easily design filters that manipulate different frequencies in signals
- We can pass the input signal through a Fourier transform to get sinusoids, which are very easy to work with in the Laplace domain with e.g. Bode plots (change of output vs. frequency), from which we can directly find the output signal of a filter
  - Bode plots can be obtained from both a theoretical design and a real circuit, and even from elements like motors that aren't circuits but behave similarly

Note

Generally, not every time domain function has a Laplace transform and not every function in the Laplace domain has an inverse. However in this course we will assume that the transforms and inverses always exist for sake of simplicity.

Poles and Zeroes

Note

Complex numbers in this course are represented as

$$s = \sigma + j\omega$$

where j is the imaginary unit, $j^2 = -1$, and σ and ω are the real and imaginary parts respectively. When we wish to represent a pure frequency, we will use only the imaginary $j\omega$, where ω is the frequency of the signal in radians/s.

- Complex functions are represented as $F(s) = F_x + jF_y$
  - F can represent a signal, or a transfer function
- A complex function $G(s)$ is *analytic* in a region if $G(s)$ if it and all its derivatives all exist; these are known as *ordinary points* and don't tell you much
  - Points where $G(s)$ is not analytic are *singular points*, which are important indicators of what the signal looks like or how the transfer function behaves

Definition

Singular points where $G(s)$ or its derivatives approach infinity are known as *poles* of the function; if $\lim_{s \to p} G(s) = \infty$ and

$$G(s)(s+p)^n$$

has a finite, non-zero value at $s = -p$, then it is a pole of order n.

Definition

Singular points where $G(s)$ or its derivatives approach zero are called *zeroes* of the function.

- Poles indicate places where the frequency response changes in a filter; e.g. where the frequency cutoff between pass and block happens
- Zeros determine behaviour indirectly by interacting with poles; they somewhat cancel out the effect of a pole
  - Using zeros, we can add zeros to change the system's behaviour
- Example: $\frac{(s+z)}{(s+p)}$ has a zero at $s = -z$ and a pole at $s = -p$
  - If z and p are far apart, the zero doesn't really do much
  - As the zero and pole get closer, they interact in the transient (short-term) domain
  - If $z = p$, the pole and zero can also cancel out
- Example: $G(s) = \frac{K(s+2)(s+10)}{s(s+1)(s+5)(s+15)^2}$
  - Note how we factored the signal into a form where the poles and zeros are easily identified
  - Poles: 5 total at $s = 0, -1, -5, -15$ (last one is order 2)
    - We will see that when poles are stacked on each other, it amplifies their effect
  - Zeroes: 2 (finite) total at $s = -2, -10$
    - Strictly speaking we will also have 3 more zeros at $s \to \pm\infty$, since the numerator is degree 2 and denominator is degree 3
  - Based on this, we can see 3 terms exponentially decaying, 1 step (constant), and some transient up-down behaviour in the signal; we can see this by looking at properties of the Laplace transform:
    - Terms that are $\frac{1}{s+\alpha}$ are exponential decay $e^{-\alpha t}$
      - Note that α has to be a purely real number for it to be exponential decay
    - Terms that are $\frac{1}{s}$ are steps
    - The poles at -1, -5, and the zero at -2 influence each other to lead to transient behaviour

Important

As a general rule of thumb, if the poles and zeros are in the same order of magnitude, they will interfere leading to transient behaviour; the closer the pole is to the zero, the greater the effect in the short term but the more they cancel in the long term.

- Note that functions that grow faster than an exponential do not have Laplace transforms since they do not converge, but we never want to analyze these functions anyway
- The linearity of the Laplace transform allows us to break time domain signals into sinusoids, which are very easy to work with
- Some common Laplace transforms:
  - A decaying exponential transforms to $\frac{A}{s+\alpha}$ where α is a positive real constant
  - A step transforms to $\frac{A}{s}$

  - A ramp function (e.g. $f(t) = t$) transforms to $\frac{A}{s^2}$
  - A sinusoid transforms to $\frac{A\omega}{s^2 + \omega^2}$
    * This means if we have a pair of poles at $s = \pm j\omega$, it corresponds to a sinusoid

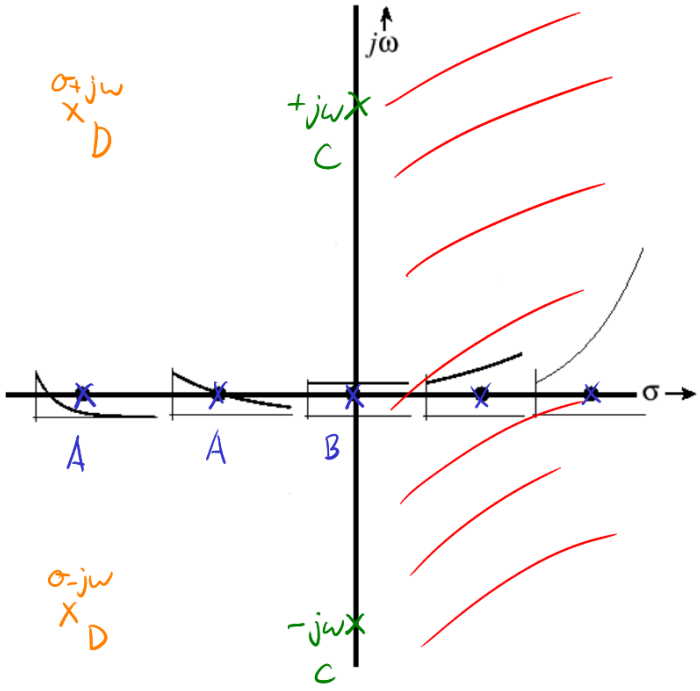

Figure 2: Poles plotted on the imaginary plane.

- Notes for the figure:
  - Poles are often marked with X on the imaginary plane
  - Points labelled A are purely real and negative, so they are of the form $\frac{1}{s + \alpha}$ which gives us exponential decay
    * The further away the pole is from zero (i.e. bigger α), the faster the decay
  - The point labelled B is of the form $\frac{1}{s}$ which gives us a unit step or constant offset
  - All points on the right are exponential growth (unstable poles), which are intangible in real circuit design, so in practice we don't care about them
  - Points labelled C are purely imaginary and come in conjugates, which are sustained oscillations (sinusoids)
  - Points labelled D have both imaginary and negative real parts, which gives us an exponentially decaying sinusoid
    * The frequency is $\sin(\omega t)$ and decay follows $e^{-\sigma t}$

Lecture 2, Sep 13, 2023

Key Properties of the Laplace Transform

- The basic impulse function is given by $g(t) = \begin{cases} \lim_{t_0 \to 0} \frac{A}{t_0} & 0 < t < t_0 \\ 0 & \text{elsewhere} \end{cases}$
  - $\mathcal{L}\{g(t)\} = A$
- Multiply by $e^{-\alpha t}$ in time domain is a shift in frequency domain

  - $\mathcal{L}\left\{e^{-\alpha t} f(t)\right\} = F(s+\alpha)$
  - By shifting the signal in the frequency domain, we introduce an exponential decay in the signal – this can be used to remove poles that we don't want to modify the steady-state behaviour
- A change of time scale in the time domain corresponds to a scaling in frequency domain
  - $\mathcal{L}\left\{f\left(\frac{t}{a}\right)\right\} = aF(as)$
  - This allows us to manipulate frequencies while keeping other important information such as phase intact
- Differentiation in time domain is equivalent to multiplication by s in the frequency domain
  - $\mathcal{L}\left\{\frac{\mathrm{d}}{\mathrm{d}t} f(t)\right\} = sF(s) - f(0)$
  - Note that if there is an impulse at $t = 0$, two separate Laplace transforms must be used
  - This allows us to implement differentiation circuits
- Final value theorem: $\lim_{t\to\infty} f(t) = \lim_{s\to 0} sF(s)$
  - To find the steady-state behaviour for a stable, settling system, we can use this limit in the frequency domain, which is often much easier to evaluate
- Initial value theorem: $\lim_{t\to 0^+} f(t) = \lim_{s\to\infty} sF(s)$
  - This can be used to find the initial conditions, provided the limit exists in the Laplace domain
- Multiplication by t in the time domain is differentiation in frequency domain:
  - $\mathcal{L}\left\{t^n f(t)\right\} = (-1)^n \frac{\mathrm{d}^n}{\mathrm{d}s^n} F(s)$
- Convolution in time domain is multiplication in Laplace domain:
  - $\mathcal{L}\left\{f_1(t) * f_2(t)\right\} = \mathcal{L}\left\{\int_0^t f_1(t-\tau) f_2(\tau)\,\mathrm{d}\tau\right\} = F_1(s)F_2(s)$
  - This can be used to easily determine the output of a system given some input signal

Circuits in Frequency Domain

- In frequency domain Ohm's law becomes $V(s) = I(s) \cdot Z$
  - The impedance Z has both real and imaginary components, unlike in normal Ohm's law
- Resistors behave the same regardless of frequency, so $Z = R$ for resistors
- However capacitors and inductors behave differently depending on frequency

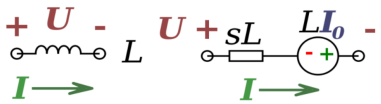

Figure 3: An inductor in time and frequency domain.

- An inductor in frequency domain is separated into two parts: the impedance $Z = sL$ for the steady-state conditions, and another part that responds to initial conditions; when we analyze steady-state behaviour, we can ignore the second part
  - $v(t) = L\frac{\mathrm{d}i(t)}{\mathrm{d}t} \implies V(s) = sLI(s) - Li(0)$
  - Notice that for DC current, $s = j\omega = 0$ so the inductor becomes an open circuit in steady state
  - For higher frequencies, s increases so the impedance also increases

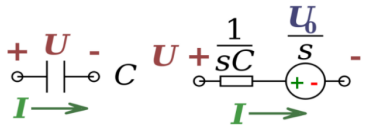

Figure 4: A capacitor in time and frequency domain.

- A capacitor similarly has impedance $Z = \frac{1}{sC}$ and another part responding to initial conditions
  - $i(t) = C\frac{\mathrm{d}v(t)}{\mathrm{d}t} \implies I(s) = CsV(s) - CV(0) \implies V(s) = \frac{1}{sC}I(s) + \frac{1}{s}V(0)$
  - For DC current, the capacitor behaves as an open circuit (infinite impedance)
  - For higher frequencies, the impedance decreases
- Any calculations that we could do with Ohm's law in time domain, we can do in frequency domain with impedances
  - This applies to techniques such as nodal analysis, mesh current, etc
  - Crucially, superposition also holds

Summary

To transform circuits into the frequency domain:
- Resistor: $Z = R$
- Inductor: $Z = sL$ plus a source with voltage $V(s) = Li(0)$ for initial conditions
- Capacitor: $Z = \frac{1}{sC}$ plus a source with voltage $V(s) = \frac{v(0)}{s}$ for initial conditions

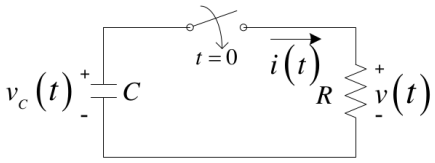

Figure 5: Example problem.

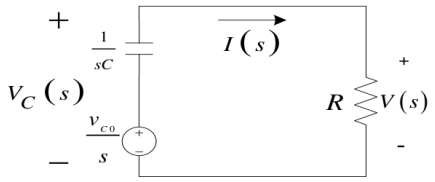

Figure 6: Example problem in frequency domain.

- Example: consider the circuit above where the capacitor is charged to a voltage of $v_c = v_{c_0}$; the switch is closed at time $t = 0$; find the resistor voltage $v(t)$
  - First transform the circuit into frequency domain as shown above; note the capacitor transforms into two sources due to initial conditions
  - $\frac{v_{c_0}}{s} - I(s)\frac{1}{sC} - I(s)R = 0$
    * Note that we're looking for $V(s) = I(s)R$
    * $I(s)\left(R + \frac{1}{sC}\right) = \frac{v_{c_0}}{s} \implies I(s) = \frac{\frac{v_{c_0}}{s}}{R + \frac{1}{sC}} = \frac{\frac{1}{R}}{s + \frac{1}{RC}}v_{c_0}$
      - Tip: to save time, avoid merging terms or normalizing until the very end
      - To normalize, we should do it so that the highest power of s in the dominator has a coefficient of 1
      - We can clearly see that there is a pole at $s = -\frac{1}{RC}$, corresponding to an exponential decay as we expected
    * Multiplying by R we get $V(s) = \frac{1}{s + \frac{1}{RC}}v_{c_0}$ so $v(t) = u(t)v_{c_0}e^{-\frac{1}{RC}t}$

Lecture 3, Sep 15, 2023

Example: Solving For Steady-State Behaviour in the Frequency Domain

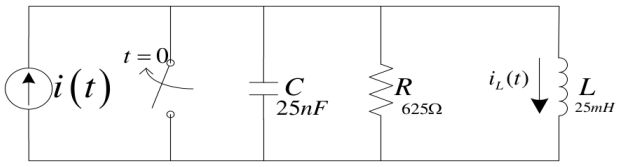

Figure 7: Example problem.

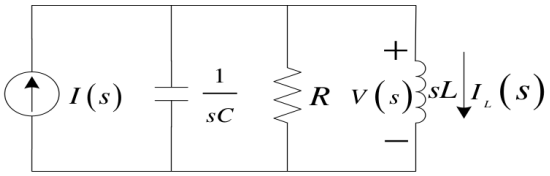

Figure 8: Example problem in frequency domain (steady state).

- Example: find the steady-state current through the inductor $i_L(t)$, given $i(t) = 24$mA (DC) and no initial conditions
  - In the long term we expect all the current to go through the inductor; let's verify this
  - In the short term we expect the capacitor and inductor to cause oscillations
  - We will first solve for the voltage across the inductor using node voltage, making the bottom node the ground
    - $i(t) = 24u(t)[\text{mA}] \implies I(s) = \dfrac{0.024}{s}[\text{A}]$
    - $-I(s) + sCV(s) + RV(s) + \dfrac{V(s)}{sL} = 0 \implies V(s) = \dfrac{\frac{0.024}{s}}{sC + R + \frac{1}{sL}}$
    - Normalize: $\dfrac{\frac{0.024}{C}}{s^2 + \frac{1}{RC}s + \frac{1}{LC}}$
      - The s^2 in the denominator gives us two possible outcomes: two real-valued poles (two pure exponential decays) or a complex conjugate pair (decaying sinusoid)
  - $I(s) = \dfrac{V(s)}{sL} = \dfrac{\frac{0.024}{LC}}{s\left(s^2 + \frac{1}{RC}s + \frac{1}{LC}\right)}$
    - The additional $\dfrac{1}{s}$ this introduces would give us a unit step
    - The overall behaviour is a sudden increase at $t = 0$ with some small oscillations, which eventually decay to just a constant DC value
    - If we sub in the values we get: $\dfrac{384 \times 10^5}{s(s + 32000 + 24000j)(s + 32000 - 24000j)}$
      - The 32000 is the rate of decay; the 24000 is the frequency of oscillation
  - To find the steady-state behaviour, we could inverse Laplace transform $I(s)$ and take the limit as $t \to \infty$, but it's much easier to use the Final Value Theorem and do it in the Laplace domain
    - $\lim\limits_{t\to\infty} i(t) = \lim\limits_{s\to 0} sI(s) = \lim\limits_{s\to 0} \dfrac{384 \times 10^5}{(s + 32000 + 24000j)(s + 32000 - 24000j)} = 0.024[\text{A}]$
    - Note that we can only do this because all the poles of $I(s)$ have negative real parts, i.e. it trends towards a steady DC value
- Example: same problem as above, but the current source is now $i(t) = (0.024)\cos(40000t)$
  - At a fixed frequency, the impedance of the capacitor, resistor, and inductor all have fixed and finite impedances, so this behaves like 3 resistances in parallel; we would expect that the shape of the signal remains the same, but its amplitude decreases

- $I(s) = \dfrac{0.024s}{s^2 + 40000^2}$
- $-I(s) + sCV(s) + RV(s) + \dfrac{V(s)}{sL} = 0 \implies V(s)\left(sC + \dfrac{1}{R} + \dfrac{1}{sL}\right) = 0.024\dfrac{s}{s^2 + 40000^2}$
- $V(s) = \dfrac{0.024}{C}\left(\dfrac{\cdots}{\left(s^2 + \frac{1}{RC}s + \frac{1}{LC}\right)\left(s^2 + 40000^2\right)}\right) = \dfrac{\cdots}{(s + 32000 \pm 24000j)\,(s \pm 40000j)}$
  - We have a combination of a sustained oscillation and a decaying oscillation
  - In the long term only the sustained oscillation will remain
- What happens if we try to apply the FVT?
  - We end up with an s^2 in the numerator after cancelling terms, so the FVT tells us it is zero
  - However we know that the long-term behaviour is a sustained oscillation, not a DC zero
  - This does however tell us the DC offset, but it is misleading
- To analyze this, we'll have to actually do the inverse Laplace transform
- In reality, since the time constant is very large for the decaying oscillation, it will decay out in only half a cycle of the sustained oscillation, so its effect is barely noticeable

Transfer Functions

Definition

A *transfer function* $H(s)$ in the frequency domain is the ratio of the output to input of a system in the Laplace domain:

$$H(s) = \frac{Y(s)}{X(s)}$$

where $Y(s)$ is the output and $X(s)$ is the input in Laplace domain.

- A transfer function captures the system's response to inputs, so if we have a transfer function, we can determine the system's response to any input
  - These can be derived from the circuit or measured by injecting a known signal
  - We can also go back from a transfer function to a practical circuit design
  - We can get the output by simply $Y(s) = H(s)X(s)$, which corresponds to a convolution in time domain
- We will restrict ourselves to circuits that are SISO (single-input, single-output); to work with MIMO systems, we need to use matrix notation
- We will also assume that $H(s)$ is time-invariant
- Crucially, if we have multiple circuits connected in series, the overall transfer function is just the product of all the individual transfer functions
  - This allows us to design circuits in blocks which drastically simplifies and speeds up design
  - Note that this assumes no loading effects!

Important

A *loading effect* happens when the transfer function of the first circuit changes due to current drawn by the second circuit. This happens when the first circuit has finite output impedance and the second circuit has finite input impedance. When there are loading effects, we cannot simply multiply transfer functions.

- Circuits made of regular passive components always have loading effects, but we can use op-amps to get rid of them
  - The ideal op-amp can drive any load, so it would have no loading effect at all
- Example: find the transfer function of the circuit above, where the output $v_{out}(t)$ is taken from the top-right node

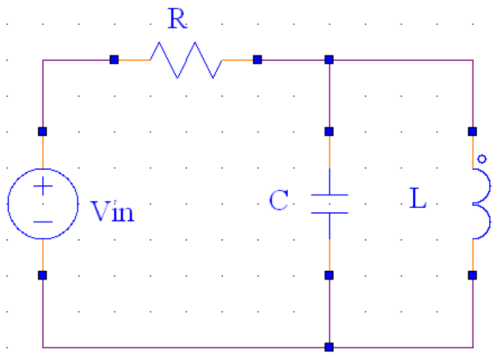

Figure 9: Example LC tank circuit.

- For the capacitor and inductor, $Z_{eq} = \dfrac{1}{\frac{1}{sL} + sC} = \dfrac{\frac{s}{C}}{s^2 + \frac{1}{LC}}$
- Now we can treat it as a voltage divider, so $V_{out}(s) = V_{in}(s)\dfrac{Z_{eq}}{Z_{eq} + R}$
- $H(s) = \dfrac{V_{out}(s)}{V_{in}(s)} = \dfrac{\frac{s}{RC}}{s^2 + \frac{1}{RC}s + \frac{1}{LC}}$
- This circuit is a *band-pass filter* – it passes only a narrow band of frequencies, and for frequencies higher or lower, it essentially eliminates them
- What happens if the output was connected to another copy of the circuit?
  * We expect loading effects to happen since the circuit is made of only passive components
  * Let $V_x(s)$ be the voltage at the output of the first circuit
  * $\dfrac{V_x - V_{in}}{R_1} + \dfrac{V_x}{\frac{1}{sC_1}} + \dfrac{V_x}{sL_1} + \underbrace{\dfrac{V_x - V_{out}}{R_2}}_{\text{loading effect!}} = 0$
  * If we solve this and compare to what we get by multiplying transfer functions, we see that the s^3 and s terms in the denominator are different

Lecture 4, Sep 20, 2023

Transfer Functions of Op-Amp Circuits

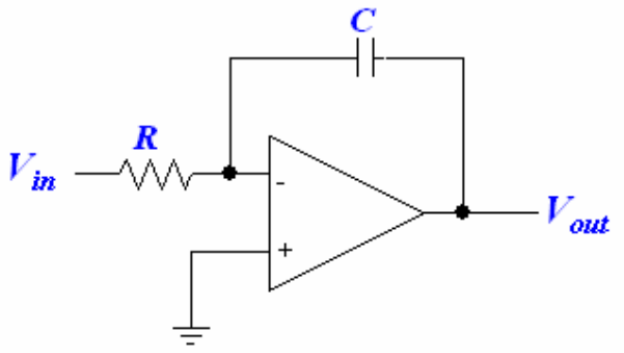

Figure 10: Example integrator op-amp circuit.

- Example: find the transfer function for the circuit above
  - As a shortcut, we can notice how this resembles an inverting amplifier, so we can use the same formula and replace the resistances with impedances

    * Recall that for an inverting amplifier $\frac{V_{out}}{V_{in}} = -\frac{R_2}{R_1}$, so in this case we have $H(s) = -\frac{Z_2}{Z_1} = -\frac{1}{sRC}$
  - If we couldn't rely on the shortcut, we must use KVL at the inverting input
    * $\frac{V_x - V_{in}}{R} + \frac{V_x - V_{out}}{\frac{1}{sC}} = 0$
    * Since there is a valid negative feedback path, we know the voltage at the inverting and noninverting inputs are equal; therefore $V_x = 0$
    * Using this, $-\frac{V_{in}}{R} - sCV_{out} = 0 \implies \frac{V_{out}}{V_{in}} = -\frac{1}{sRC}$
  - We couldn't have used KVL at the output node, because the op-amp has a current output that we do not know
  - Since multiplying a signal by $\frac{1}{s}$ in the frequency domain is equivalent to an integration (because multiplication by s is differentiation), this circuit is an integrator for the input signal
  - Note: in practice, capacitors don't hold their charge perfectly; since the capacitor is effectively keeping track of the integration state, the capacitor leaking charge leads to errors; in addition, real noise is often not zero-mean, so noise in the signal may accumulate

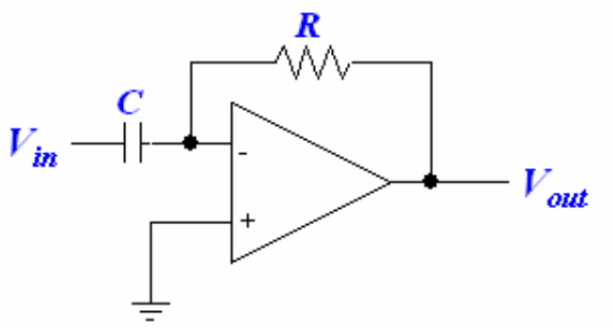

Figure 11: Example differentiator op-amp circuit.

- Example: find the transfer function for the circuit above
  - $H(s) = -\frac{Z_2}{Z_1} = -\frac{R}{\frac{1}{sC}} = -sRC$
  - Multiplication by s is a differentiation in time domain, so this circuit is a differentiator
  - Note that this and the integrator are frequency limited; they may not respond properly with very high frequencies
- When there are multiple inputs, we can find the transfer functions for each input separately; however we have to assume that the other inputs are at some fixed known voltage, usually zero
- Example: find the transfer function for the circuit above
  - Notice that we can break this into the 4 individual op-amp circuits: the inverting amplifier U_1, the integrator U_2, the differentiator U_3, and summing amplifier U_4; we will find transfer functions for each one individually and combine them
  - Note: this is a PID circuit, where an input error is scaled, integrated, and differentiated, and then combined together to form the control output
  - $H_1(s) = -\frac{R_2}{R_1}, H_2(s) = -\frac{1}{sR_3C_1}, H_3(s) = -sR_4C_2$
    * Note our assumptions: no loading effects at the input or output
  - For the summing amplifier, $Y(s) = -\left(\frac{R_8}{R_5}A(s) + \frac{R_8}{R_6}B(s) + \frac{R_8}{R_5}C(s)\right)$
  - Therefore $H(s) = \frac{Y(s)}{E(s)} = \frac{R_2R_8}{R_1R_5} + \frac{R_8}{R_3R_6C_1}\frac{1}{s} + \frac{R_4R_8C_2}{R_7}s$

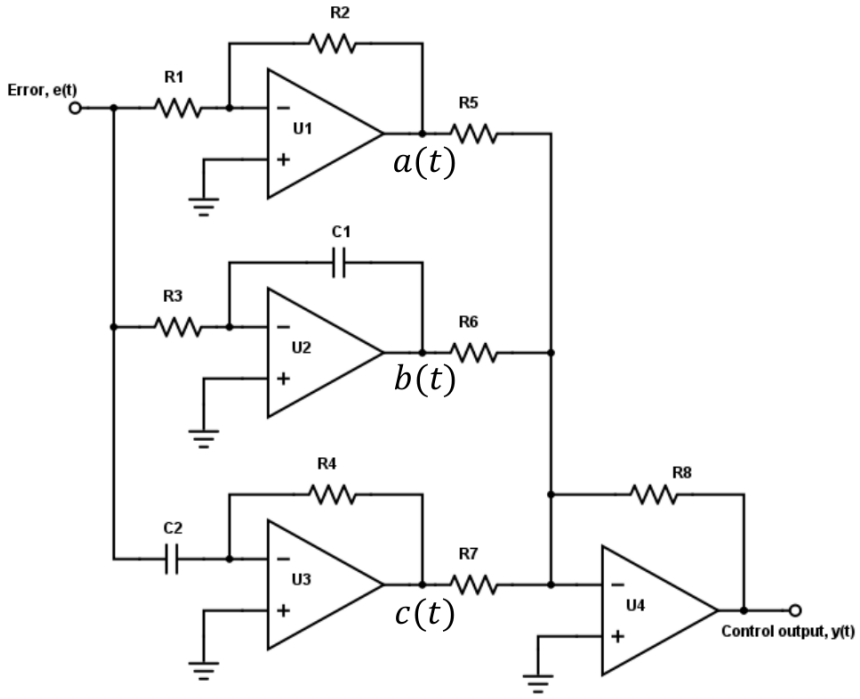

Figure 12: Example PID control loop circuit.

– Bringing this back to the time domain, we have $y(t) = K_P e(t) + K_I \int e(t)\,\mathrm{d}t + K_D \frac{\mathrm{d}}{\mathrm{d}t} e(t)$

Lecture 5, Sep 22, 2023

Analyzing Complex Op-Amp Circuits

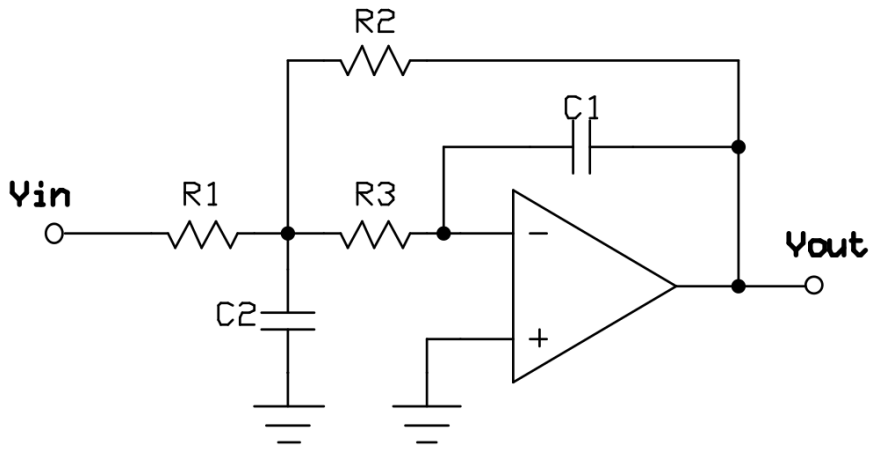

Figure 13: An inseparable op-amp circuit.

- Example: find the transfer function of the above circuit
  - There is only one op-amp so we can't break this circuit down; we must write multiple node equations
  - We should write node equations at the inverting input (V_y) and the node to the right of V_{in} (V_x)

    * We also know that $V_y = 0$
  - $\frac{V_x - V_{in}}{R_1} + sC_2V_x + \frac{V_x - V_{out}}{R_2} + \frac{V_x}{R_3} = 0 \implies \left(sC_2 + \frac{1}{R_1} + \frac{1}{R_3} + \frac{1}{R_2}\right)V_x + \left(-\frac{1}{R_1}\right)V_{in} + \left(-\frac{1}{R_2}\right)V_{out} = 0$
  - $\frac{-V_x}{R_3} + -sC_1V_{out} = 0 \implies V_x = -sR_1C_3V_{out}$
  - Sub back to get $H(s) = \frac{\left(\frac{1}{R_1}\right)}{-s^2C_1C_2R_3 + \left(-\frac{C_1R_3}{R_1} - C_1 - \frac{C_1R_3}{R_2}\right)s + \left(-\frac{1}{R_2}\right)}$
    * Normalize: $-\frac{\frac{1}{C_1C_2R_1R_3}}{s^2 + \left(-\frac{1}{C_2R_1} + \frac{1}{C_2R_2} + \frac{1}{C_2R_3}\right)s + \left(\frac{1}{C_1C_2R_2R_3}\right)}$

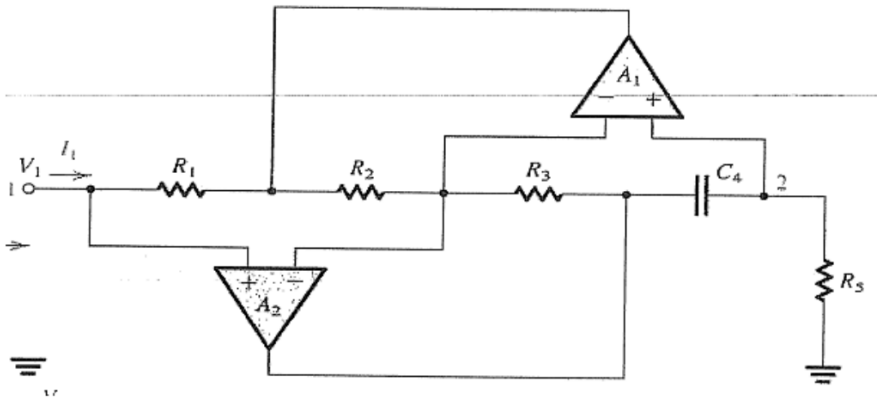

Figure 14: Example circuit to find the equivalent impedance.

- Example: find the equivalent input impedance of the circuit above
  - We want to find an input current I_{in} caused by an input voltage V_{in}, then we can find the impedance as $\frac{V_{in}}{I_{in}}$
  - Note we can't write useful node equations at the node between R_1, R_2 or the node between R_3, C_4 because they are both connected to the output of op-amps
  - The node between R_2, R_3 and the node between C_4, R_5 have the same voltage as V_{in} due to the op-amp feedback
  - Node equations:
    * $\frac{V_{in} - V_A}{R_1} - I_{in} = 0 \implies V_A = V_{in} - R_1I_{in}$
    * $\frac{V_{in} - V_A}{R_2} + \frac{V_{in} - V_C}{R_3} = 0 \implies V_{in}\left(\frac{1}{R_2} + \frac{1}{R_3}\right) + V_A\left(-\frac{1}{R_2}\right) + V_C\left(-\frac{1}{R_3}\right) = 0 \implies V_C = V_{in} - \frac{R_1R_3}{R_2}I_{in}$
    * $sC_4(V_{in} - V_C) + \frac{V_{in}}{R_3} = 0 \implies -\frac{sC_4R_1R_3}{R_2}I_{in} + \frac{1}{R_5}V_{in} = 0$
    * $Z_{eq} = \frac{V_{in}}{I_{in}} = s\left(\frac{C_4R_1R_3R_5}{R_2}\right)$
  - If we let $\frac{C_4R_1R_3R_5}{R_2} = L$, we see $Z_{eq} = sL$ – this circuit is an inductance simulator
  - Inductors are very hard to work with at a small scale, so circuits like these are often used to replace inductors with other components
  - Note this only simulates the frequency response of an inductor, but not other aspects like the energy storage

Real-World Op-Amps

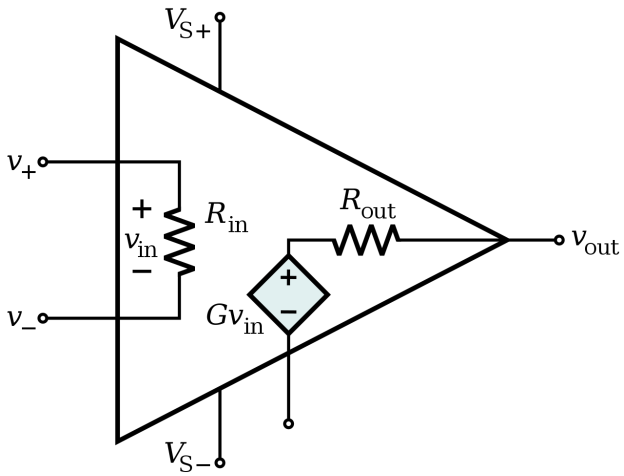

Figure 15: Equivalent internal model of a real-life op-amp.

- Real-world op-amps have several differences compared to ideal op-amps:
  1. Feedback loops: the degree of negative feedback (output to inverting input) must be greater than the degree of positive feedback (output to noninverting input) for the system to be stable
     - For our purposes, we assume that the feedback is sufficient as long as there is a path from the output to the inverting input
  2. Finite input impedance: the impedance looking into the terminals is finite, which means that a small current can flow into the inputs
     - This impedance is frequency dependent but most of the time it suffices to model as a simple resistance
     - The input impedance is often in the range of megaohms to gigaohms, even for cheap op-amps
     - In most cases, the assumption that no current flows in is valid, unless the external resistances attached are on the same order of magnitude (or greater) than the internal resistance
  3. Nonzero input offset: the difference between the voltages on the terminals is nonzero due to the finite open-loop gain
     - This is often in the range of millivolts or nanovolts, so it will not affect the circuit in most cases
     - This does not matter most of the time, but for particular sensitive circuits or filters it needs to be accounted for
  4. Finite open-loop gain: the op-amp output voltage is $v_{out} = (v_+ - v_-)A_0$ where A_0 is the open-loop gain; in a real-world op-amp, this gain is finite
     - This means that the feedback control is not perfect, and so the difference between the voltages of the two inputs is nonzero
     - In modern op-amps, the gain is often around 100,000 for cheaper modern op-amps, or up to millions for better ones
       * For older technology this could be in the thousands
     - To see if this will have an impact, we need to compare the op-amp gain to the function of the circuit we're trying to implement
       * e.g. if we're trying to make an inverting amplifier, and the gain we want is within an order of magnitude of the open-loop gain, then it could be problematic
  5. Finite bandwidth, conditional stability, and not linear time-invariant (LTI): real op-amps can be frequency-limited, can have stability issues, and may not be perfectly linear time-invariant
     - The bandwidth is usually limited to megahertz to gigahertz ranges
     - The op-amp should be at least an order of magnitude faster than the operating range of the circuit

6. Nonzero output impedance: the impedance of the output is nonzero, so the amount of current we can draw is finite
   - Drawing too much current would start causing considerable loading effects
   - The output resistance is typically in the range of ohms to kilohms
   - Since we're usually using kilohm-level resistances in our circuits, this could be a very common issue

- Additionally, real-world op-amps must be powered by some pair of voltages V_{dd}, V_{ss}, which restricts the range that V_{out} can take on
  - If we expect the output voltage to be outside this range, it is capped instead
  - When the waveform is cut off due to op-amp output limits, it is referred to as *clipping*
  - Clipping may not happen right at the supply voltage; there may be a small gap and clipping happens slightly below the supply voltage

Lecture 6, Sep 27, 2023

Bode Plots

- Motivation: we need a good tool to predict what a circuit will do to a wide range of signal frequencies
- Example: $H(s) = \dfrac{1}{Ts+1}$ with $y(t) = A\sin(\omega t)$
  - We will always get a sine wave of the same frequency
  - However the phase and the amplitude of the output will be different
  - In general, all LTI systems have this property
- A Bode plot shows, for different frequencies in logarithmic scale, how a system changes the phase and amplitude of an input sinusoid
  - The information from both parts of the Bode plot are equivalent to all the information from the transfer function/pole-zero plot

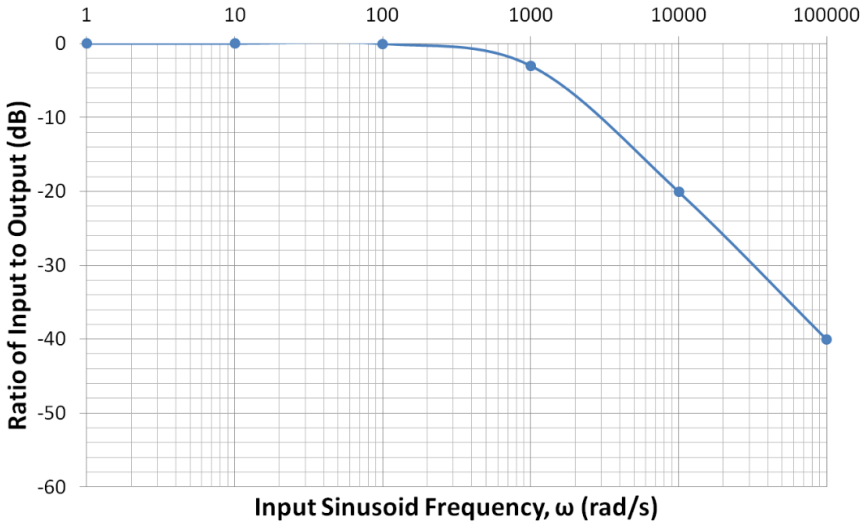

Figure 16: Magnitude Bode plot for the example transfer function.

- For the magnitude plot, a Bode plot shows the ratio of output amplitude over input amplitude in decibels – $\text{dB} = 20\log_{10}\dfrac{A_{out}}{A_{in}}$
  - At -3dB, we consider the output amplitude to have started deviating considerably
  - A typical Bode plot for a single pole looks similar to the example figure, with a horizontal segment where frequency has little effect, and a diagonal segment where increasing frequency significantly affects the output

    * The inflection point is the location of the pole; this is known as the *cutoff frequency* or *corner frequency*
    * After the pole location, each decade of increase in frequency leads to about -20dB of amplitude difference

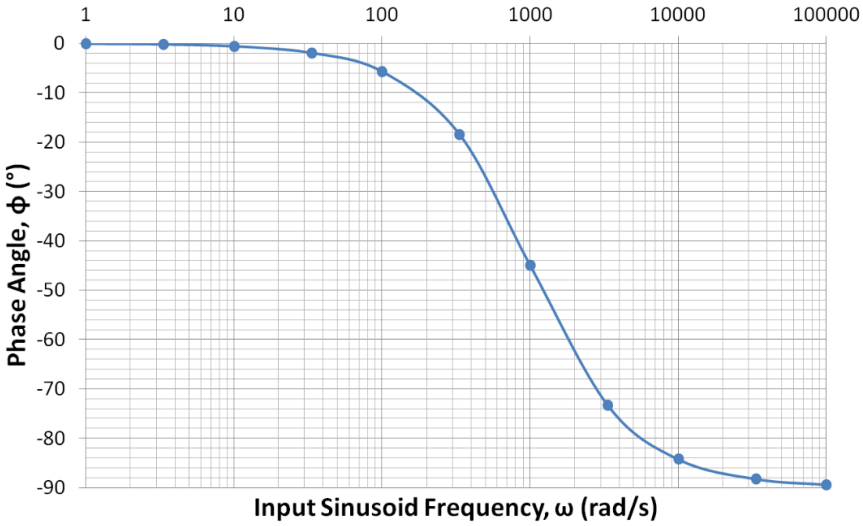

Figure 17: Phase Bode plot for the example transfer function.

- For the phase plot, the phase shift angle in degrees is shown
  - The phase plot can be approximated by 3 segments, with 2 horizontal ones and a diagonal one
  - In the diagonal segment, the phase decreases by $-45°$ per decade
  - The pole location is at the center of the diagonal segment of the phase plot; it has a phase shift of $-45°$
- A complete Bode plot requires both a magnitude and a phase plot

Lecture 7, Sep 29, 2023

Sketching Bode Plots

- Many common software tools exist to create Bode plots, but we are interested in sketching them by hand since this allows us to go from desired behaviour back to circuit
- Note that the behaviour that we discussed previously is for a single pole; if there are multiple poles/zeroes, their effects add together
- Since the horizontal axis is logarithmic, the zero frequency would be infinitely to the left
  - If our pole is at $\omega_c = 0$, the cutoff frequency would be off the plot, so we only see a diagonal line of -20dB per decade
  - The same goes for the phase plot; we almost always have a $-90°$ shift since the diagonal section is mostly off the plot
  - For such a pole we have exactly 0dB at $\omega = 1$ so we can draw a line through this point with the slope
- Zeros are effectively the opposite of poles
  - For a zero at origin, we now have a constant slope of $+20$dB per decade for the magnitude plot and a $+90°$ phase shift always
  - Compared to a pole, the effect of a zero is effectively the same as a pole but reflected across the 0dB/0° lines

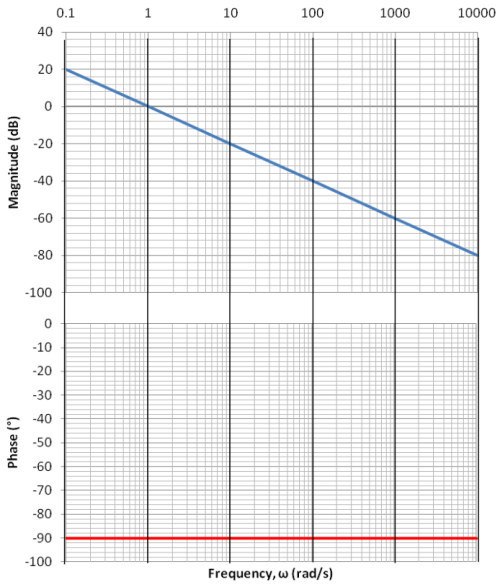

Figure 18: Bode plot for a pole at zero frequency.

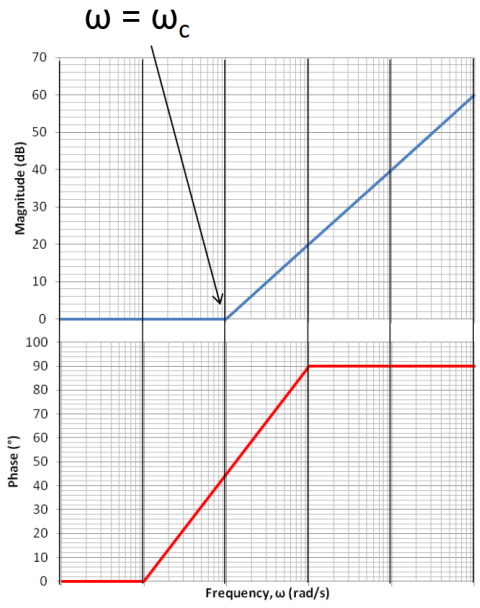

Figure 19: Bode plot for a zero.

- Note that for a phase shift the vertical axis wraps around ($360° = 0°$); by convention we try to keep it near zero
- In the case of constant gain $\pm K$, on the magnitude plot we have a constant value of $20 \log_1 0(|K|)$, but the phase plot is either a constant $0°$ if $K > 0$ or $\pm 180°$ if $K < 0$, since an inversion is equivalent to a $180°$ phase shift

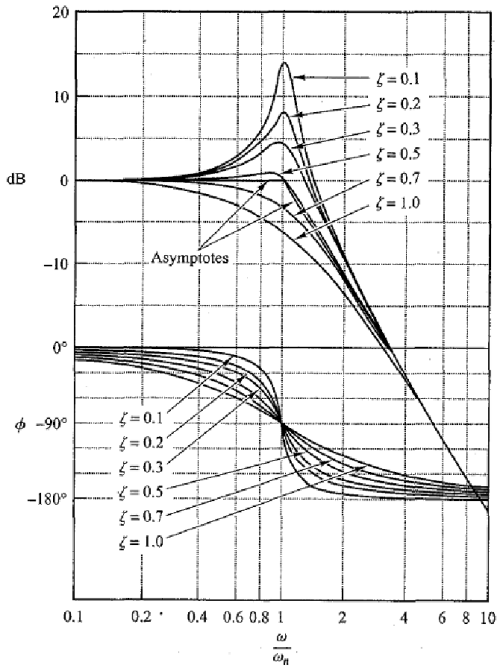

Figure 20: Bode plot for underdamped poles.

- In the case of underdamped poles and zeroes, we have a quadratic factor in the transfer function so the Bode plot is much more complicated
  - We will not deal with this much in this course, but be aware that our linear approximations will no longer work
  - These poles mostly have no change at lower frequencies and gives -40dB per decade at higher frequencies (which corresponds to the fact that they factor into two poles)
  - For the phase plot the total phase shift is $-180°$ at higher frequencies (since each pole contributes $-90°$); however the slope and shape of the phase plot changes significantly depending on the value of ζ
  - However at frequencies near ω_n (the natural frequency) we hit a peak, which increases as ζ (the damping factor) decreases; this corresponds to a resonance
  - For the magnitude plot we will have to split it into 3 or 4 segments to accommodate the peak
- Our linear approximation will not exactly match the real plot; we can attempt to correct for this error
  - For the magnitude plot, we can apply a correction of ± 3dB per pole at $\omega \approx \omega_c$ and ± 1dB at $\omega \approx 2^{\pm 1}\omega_c$
    - We can also use a correction graph but this is often not needed
  - For the phase plot, near $\omega = \pm 2^{\pm 1}\omega_c, |\phi| = 26.6°$ or $63.4°$; at $\omega \approx 10^{\pm} 1\omega_c, |\phi| = 5.7°$ or $84.3°$
- To graph a Bode magnitude plot by hand:
  1. Factor the transfer function into distinct poles and zeroes
     - If we can't do this then the system is probably not LTI, or if there are complex poles, it will be very difficult for us to do
  2. Determine the starting point of the graph: we want the graph to start at around a factor of 10 smaller than the smallest (nonzero) pole/zero
     - This allows us to avoid most of the error at the start of the graph; since the entire graph is

going to be relative to this point, if we have errors at the start the entire graph will be shifted
  - Now we need to determine the start gain in decibels
  - If poles and zeros are at at least 10rad/s and we are starting at 1rad/s, we can simplify this to $K_{start} = |K| z_1 z_2 \cdots \frac{1}{p_1} \frac{1}{p_2} \cdots$, i.e. the product of all the poles and zeros
    * This works because at 1rad/s, poles and zeroes at a frequency of zero contribute nothing to the magnitude
    * We need other poles and zeros to be much bigger than 1 so our approximation works
  - Otherwise, we must sub in $s = j\omega$ manually for the starting ω and work out the initial magnitude by brute force calculations
  - Remember to convert K_{start} back to decibels!
3. Begin drawing at K_{start} (in decibels)
  - If we've picked our starting frequency properly, then we should be in the flat region of all nonzero poles and zeros
  - If there are no zero poles and zeros we start directly at this frequency, otherwise we account for them
4. Draw a straight line to the next corner frequency using the current slope
5. Update the rate of change based on which poles and zeros are active, and then repeat until we finish all segments
  - For each zero that's active, add +20dB per decade; for each pole add −20dB per decade

- The phase plot can be graphed in a similar way:
  1. Factor the transfer function into distinct poles and zeroes
  2. Determine the starting point of the graph
  3. Group and sort all corner frequencies
    - Instead of the ω_c themselves, take $0.1\omega_c$ and $10\omega_c$ which corresponds to the start and end points of the influence of each pole and zero
  4. Begin drawing at the starting point
    - Note each pole or zero at the origin will introduce a constant $\mp 90°$ shift
  5. Draw the line segments and update the rate of change
    - Each pole or zero introduces a $\mp 45°$ per decade on the rate of change and contributes $\mp 90°$ in total
    - To check, count the number of poles and zeros and make sure that the endpoint is exactly $90°z - 90°p$ from the starting point, where z is the number of zeros and p is the number of poles

- Example: Graph the Bode plot for the transfer function: $H(s) = \dfrac{s^2 + 10010s + 100000}{s^2 + 1000s}$
  - First we graph the magnitude plot:
    1. Factor the transfer function: $H(s) = 1\dfrac{(s+10)(s+10000)}{s(s+1000)}$
      * We have 2 real poles (with one at the origin), 2 real zeros, and a positive pure gain
      * Since there is an equal number of poles and zeroes their effect cancels in the long term
    2. Find the initial magnitude: $K_{start} = (1)\left(\dfrac{1}{1}\right)\left(\dfrac{1}{1000}\right)(10)(10000) = 100 \implies K_{start_{dB}} =$ 40dB and the starting point, which we choose to be 1rad/s which is a decade below the smallest pole/zero
      * Since the gain is positive we don't need to start with a $-180°$ phase
      * The starting slope is not flat but −20dB per decade since we have a pole at the origin
      * Since we start at $\omega = 1$ the pole at origin does not affect the starting magnitude
      * We can also use the shortcut to compute K_{start} which would not have been possible if we started at some other frequency
    3. Group the poles and zeros:
      * $\omega = 0$; pole at origin; −20dB per decade
      * $\omega = 10$; zero; flat slope after this
      * $\omega = 1000$; pole; −20dB per decade after this

    * $\omega = 10000$; zero; flat slope after this
  4. Draw all segments of the plot
- See figures below for the completed plot; notice that it is fairly similar to the exact plot, except at the corner frequencies
- Now for the phase plot:
  1. Factor the transfer function in the same way
  2. Find the starting phase shift and starting frequency
     * A positive starting gain would normally correspond to a 0° starting shift, but we have a pole at the origin, so we start at $-90°$
     * For this plot we shouldn't start at 1rad/s anymore, because the zero at $\omega_c = 10$ generates two inflection points at 1 and 100rad/s
  3. Organize the poles and zeros and their effects:
     * $\omega = 0$; pole at origin
     * $\omega = 1$; start zero at $\omega = 10$
     * $\omega = 100$; end zero at $\omega = 10$ and start pole at $\omega = 1000$
     * $\omega = 1000$; start zero at $\omega = 10000$
     * $\omega = 10000$; end pole at $\omega = 1000$
     * $\omega = 100000$; end zero at $\omega = 10000$

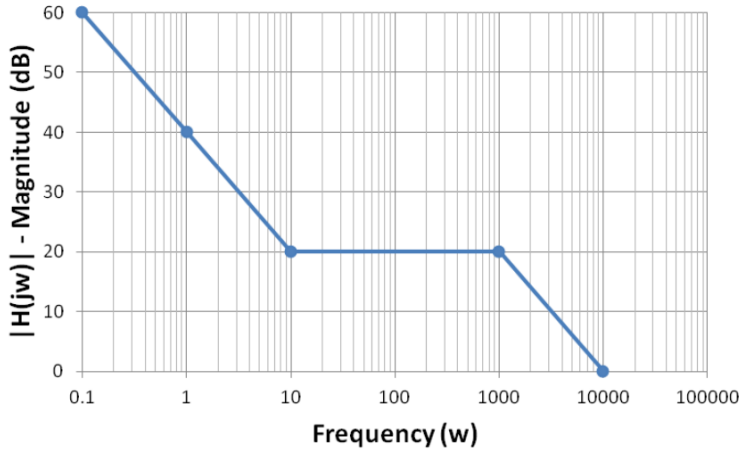

Figure 21: Magnitude plot for the example transfer function.

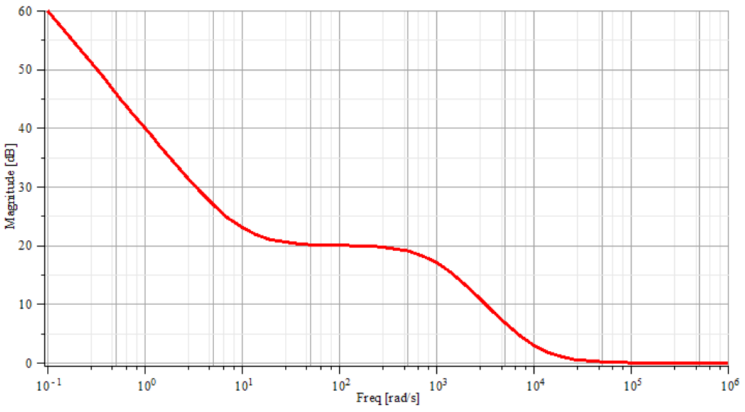

Figure 22: Exact magnitude plot created in Maple.

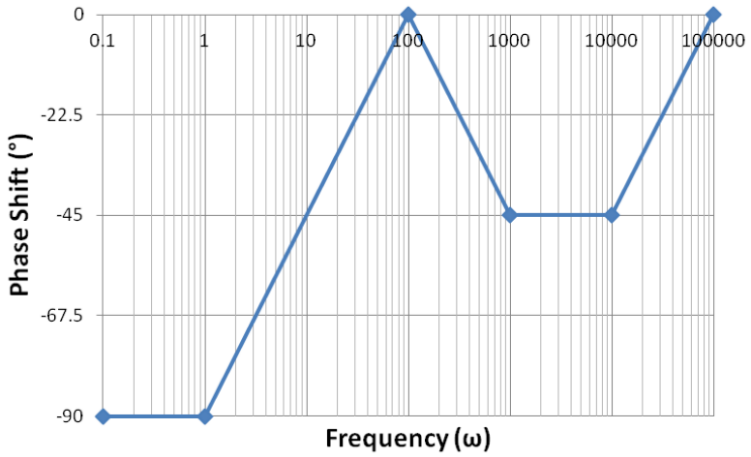

Figure 23: Phase plot for the example transfer function.

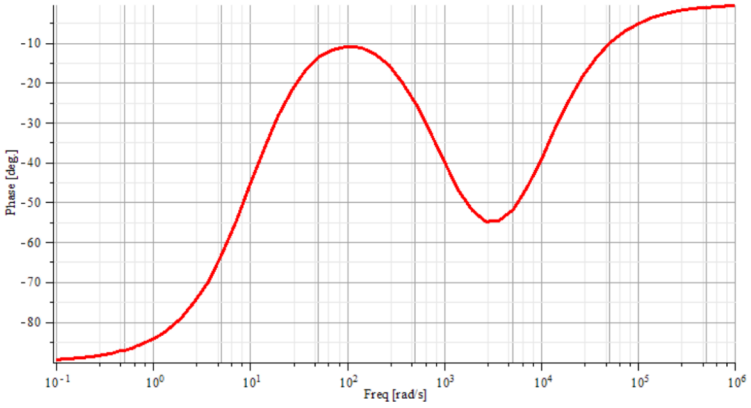

Figure 24: Exact phase plot created in Maple.

Lecture 8, Oct 4, 2023

Bode Plot Example

- $H(s) = -\dfrac{s(s+100)(s+10000)}{(s+10)(s+500)(s+1000)}$
- Note the phase plot will be a bit more complex since the negative sign introduces a 180° phase shift
- For the magnitude plot:
  - Since the smallest pole/zero is at 10, we can use the simplification to find the initial magnitude
    * $K_{start} = (1)\dfrac{(100)(10000)}{(10)(500)(1000)} = \dfrac{1}{5} = -14\text{dB}$
  - The starting slope is +20dB per decade from the single zero at zero frequency
- For the phase plot:
  - The starting phase shift is 90° from the zero at the origin, plus or minus 180° due to the negative sign; we will choose −90°

Lecture 9, Oct 6, 2023

From Bode Plot to Transfer Function

- We can reverse a Bode plot back into a transfer function by examining the magnitude plot:
  - Start by looking at the graph and finding all the inflection points – these are the pole and zero corner frequencies
  - Reverse the change in slope to find the multiplicities of the poles/zeroes
  - Check for poles and zeros at the origin
  - Pick any point on the graph, and use this to solve for the pure gain on the transfer function
  - Note if we started with an exact bode plot, we have to first estimate the asymptote plot (however this is relatively rare since reversing a bode plot is often used as a design tool)
- However, if we only look at the magnitude graph, we do not get a unique solution – there are multiple transfer functions that will give you the same magnitude plot, but not the same phase plot
  - Most of the time we don't care about the phase change when working with filter design
  - This could matter a lot in e.g. control systems
  - It also limits us to systems with magnitude rates of change being multiples of 20dB per decade; transfer functions with complex components can be problematic

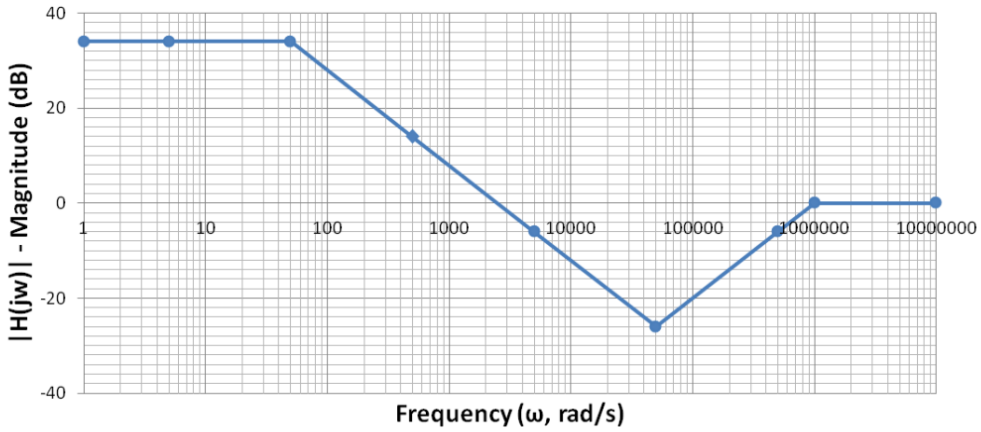

Figure 25: Phase plot for the example problem.

- Example reverse the Bode phase plot above:
  - We see inflection points at 50, 50k, and 1M, which are the corner frequencies
  - At 1M, the slope changes from +20dB per decade to 0, so a pole with multiplicity 1 became active

- At 50k, the slope changes from -20dB per decade to $+20$dB per decade, so a zero with multiplicity 2 became active
- At 50, the slope changes from 0 to -20dB per decade, so a pole with multiplicity 1 became active
- We started with a flat slope, so there is no pole or zero at the origin
- Therefore the transfer function has form $\dfrac{|K|(s+50000)^2}{(s+50)(s+1000000)}$
- At $\omega = 1$ the magnitude plot has value 34dB $= 50.119$; in our transfer function we have $|K|(50000)^2\left(\dfrac{1}{50}\right)\left(\dfrac{1}{1000000}\right) = 50K$
  * Note we could choose this because the first corner frequency is more than a decade greater
- Therefore $|K|$ is about 1, so $H(s) = \dfrac{(s+50000)^2}{(s+50)(s+1000000)}$
  * Note that we could've set $K = \pm 1$ and we would get the same magnitude; this would be reflected in the phase plot

From Transfer Function to Circuit

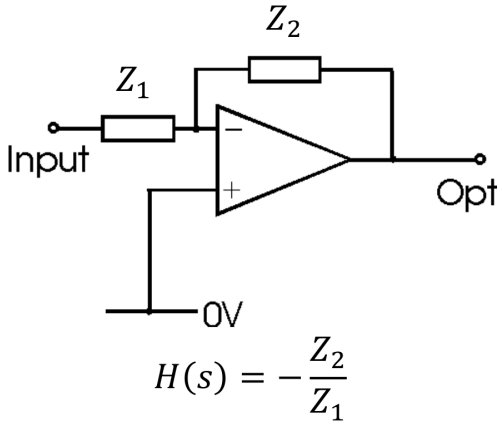

Figure 26: The inverting amplifier as a building block.

- Due to our simplifications, the simplest way for us to do this is to use a bunch of op-amp building blocks
  - Note this is an easy way, but not an optimal way
- Each inverting amplifier can (usually) give us up to one pole and one zero
- To get the desired Z_1, Z_2 to make the poles, we can choose a resistor and either an inductor or a capacitor
  - In practice capacitors are preferred because they are much cheaper and available in a wider range of values
  - However capacitors have a shorter lifespan (tens of thousands of hours vs. decades for inductors)
  - Capacitors are better at the lower frequencies while inductors are better at higher frequencies
  - In addition, we can also do resistors and capacitors/inductors in series or parallel, giving us a total of 4 choices per impedance
    * This means 16 possible combinations! Some of these can implement more advanced functions such as double poles/zeros
  - Example combination:
    * Both resistor and capacitor in series: $Z_1 = R_1 + \dfrac{1}{sC_1}, Z_2 = R_2 + \dfrac{1}{sC_2}$, then the transfer function has a pure gain of $K = -\dfrac{R_2}{R_1}$, a pole at $\dfrac{1}{R_1C_1}$, and a zero at $\dfrac{1}{R_2C_2}$
    * Both resistor and inductor in series: $Z_1 = R_1 + sL_1, Z_2 = R_2 + sL_2$, then the transfer function

has a pure gain of $K = -\frac{L_2}{L_1}$, a pole at $\frac{R_1}{L_1}$ and a zero at $\frac{R_2}{L_2}$

- In the real world, we need to choose realistic component values:
  - Resistors from 100Ω to 4.7MΩ
    - Too low and we'll get opamp loading effects
    - Too high and there will be current going into the opamp
  - Capacitors from 10pF to 1µF
    - Too low and it will be too hard to make and too sensitive (capacitance exists between rows on a breadboard!)
    - Too high and we'll have to use electrolytic capacitors, which are polarized, and less accurate
  - Inductors from 1µH to 500mH
    - Too low and the inductance will be comparable to PCB traces, so the circuit will be extremely sensitive
    - Too high and the inductor will be too hard to make and too big
- Systematic procedure to find a circuit:
  1. Group poles and zeros into pairs; each pair uses an inverting amplifier block
     - Try to keep the corner frequencies of the poles and zero close
     - When poles and zeros are very different, the gain will be extreme and reduces flexibility
     - For any remaining lone poles and zeros, add another amplifier block
  2. Divide any pure gain among the blocks; add additional pure gain blocks as needed
     - We can estimate the amount of gain that a stage provides by dividing the zero by the pole, so we can get an estimate of how much gain is left
     - Remember that real opamps have gain limits
  3. Select realistic component values
     - Start with capacitors and inductors first because they have a much smaller range of values
- Example: $H(s) = \frac{(s+50000)^2}{(s+50)(s+1000000)}$
  - We have to match one 50k zero with the 50 pole and the other 50k zero with the 1M pole
  - The first stage has a gain of approximately 1000, the second has a gain of 1/100, which leaves us with a gain of 10
    - When the leftover gain is one or two magnitudes, we are usually able to divide it among all the stages without having to add an additional amplifier
    - Note in practice we need to keep track of the magnitude of our signal in-between stages; if the signal becomes too small, it can get lost among the noise; if it's too big, it can get clipped
      - We might want to shuffle around the stages; e.g. if we have 2 stages with really big gain and 2 stages with really small gain, we should alternate the big and small gains so the signal does not get lost or clipped
  - If we have more freedom in grouping poles and zeros, we can try to group them differently in order to reduce the leftover gain
  - Lower frequency poles and zeroes are more easily realized with capacitors; higher frequency poles and zeros are more easily realized with inductors (this is a direct result of the range of component values we can use)
  - In the real world we might want to calculate the equivalent impedance of each stage of the circuit to prevent loading effects
  - For now we will try using only resistors and capacitors, by RC series
  - $H_1(s) = K_1\frac{(s+50000)}{(s+50)}, H_2(s) = K_2\frac{(s+50000)}{(s+1000000)}$ so $K_1K_2 = 1$ which is our constraint
    - We can try to get K_1, K_2 as close to 1 as possible for both stages
  - For circuit 1: we can try to select C_1, C_2 first
    - We want $\omega_c = 50$rad/s which has value $P = \frac{1}{R_1C_1}$
    - We can try a capacitor value that's in the middle of the range, e.g. 0.5µF, giving $R_1 = 43$kΩ
  - For circuit 2: let's pick $R_2 = R_1$
    - We get a capacitor value around 23pF, which works but is quite small

Important

Lower frequency poles and zeroes are more easily realized with capacitors; higher frequency poles and zeros are more easily realized with inductors. This is a direct result of the range of component values we can use. Inductors begin to struggle below 100.

Lecture 10, Oct 11, 2023

Circuit From Transfer Function Example

- $H(s) = -\dfrac{s(s+100)(s+10000)}{(s+10)(s+500)(s+1000)}$
- Note the features:
  - Zero at the origin
  - Negative pure gain with $|K| = 1$, so $|K_1||K_2||K_3| = 1$, therefore we need an odd number of inverting op-amp stages
    - Note if we only care about matching the magnitude plot, then the negative sign doesn't matter for us
- Group the poles and zeros into the 3 stages:
  - Note we want to group them so that the distance between the pole and zero is minimized in each pairing
  - $H_1(s) = K_1\dfrac{s}{s+10}, H_2(s) = K_2\dfrac{s+100}{s+500}, H_3(s) = K_3\dfrac{s+10000}{s+1000}$
  - Splitting the pure gains among the stages, we want to keep the gain of each stage close to 1
- First stage: $H_1(s) = K_1\dfrac{s}{s+10}$
  - Note if we try an RC series combination, we will have a zero at $\dfrac{1}{R_1C_1}$; to achieve a zero at the origin, we need an infinite R_1, which means the signal cannot get through
    - Note we could still use RC parallel
  - Try an RL series combination: $H(s) = -\dfrac{L_2}{L_1}\dfrac{s+\frac{R_2}{L_2}}{s+\frac{R_1}{L_1}}$
    - $\dfrac{R_2}{L_2} = 0 \implies R_2 = 0$, i.e. R_2 will be a short; L_2 can be chosen freely, so we can match it with L_1 to achieve a gain of 1
    - $\dfrac{R_1}{L_1} = 10$ but this is unachievable!
      - Note if we try our largest possible inductor of 500mH, it would still require a resistor as small as 5Ω, which is outside our range
      - The small resistor means a very low input impedance in this stage, which could lead to considerable loading effects on whatever input goes into this stage
    - Note we could have anticipated this since 10 is a relatively small pole location, so a capacitor would do better (whereas an inductor would do better for a higher frequency pole)
    - To fix this, we could:
      - Try a more complex combination of RLC (i.e. mixing up inductors and capacitors in the feedback/input path); this is the most optimal but complex
      - Break this into two stages; this is a valid on a test but is suboptimal
      - Change the matching of poles and zeroes (swapping the pole at 10 with a higher frequency one)
    - e.g. we can swap the pole at 10 with a pole at 500
      - $H(s) = \dfrac{s}{s+500}$
      - $\dfrac{R_1}{L_1} = 500 \implies L_1 = 200\text{mH}, R_1 = 100\Omega$, which is marginally acceptable

        - Choose $L_2 = L_1 = 200\text{mH}$ so this stage has a pure gain of -1 (note we can come back and pick another value later to balance out the gains)
        - In reality, we should probably use the pole at 1000 instead so we can get less extreme values
- Second stage: $H_2(s) = K_2 \dfrac{s+100}{s+10}$ (note we swapped in the pole from the previous stage)
    - The low frequency pole is difficult to realize with any RL combination, so we will use an RC combination
    - Using RC series: $H_2(s) = \dfrac{R_4}{R_3} \dfrac{s + \frac{1}{R_3 C_3}}{s + \frac{1}{R_4 C_4}}$
        * $\dfrac{1}{R_3 C_3} = 100 \implies C_3 = 0.1\mu\text{F}, R_3 = 100\text{k}\Omega$
        * Try setting $R_4 = R_3 \implies \dfrac{1}{R_4 C_4} = 10 \implies C_4 = 1\mu\text{F}$
- Third stage: $H_3(s) = K_3 \dfrac{s+10000}{s+1000}$
    - In this case both the zero and pole are near the range where capacitors and inductors work well
    - Use RC series again: $H_3(s) = \dfrac{R_6}{R_5} \dfrac{s + \frac{1}{R_5 C_5}}{s + \frac{1}{R_6 C_6}}$
        * $C_6 = 1\text{nF}, R_6 = 100\text{k}\Omega$
        * $R_5 = R_6 = 100\text{k}\Omega \implies C_5 = 10\text{nF}$
- Since each stage has a pure gain of 1, the overall gain is 1, which matches what we need; moreover, since we used an odd number of stages, we also matched the negative sign
- It's good to draw out the circuit at the very end to check for problematic open circuits and shorts, or extreme gains or attenuations

Lecture 11, Oct 14, 2023

Introduction to Diodes

- The diode is our first *active* semiconductor device, i.e. a component with a nonlinear relationship between V and I
- Diodes have two principal states, *forward* or *reverse bias* (i.e. on/off)
    - A diode passes currents in forward bias and blocks currents in reverse bias
    - A forward bias has higher voltage at the anode than the cathode and current flows in this direction
- Made of semiconducting silicon which are doped to create positive (P-type) or negative (N-type) charge carriers, forming a PN junction
    - Both P-type and N-type materials have low resistance on their own
    - In the interface between the two regions, we have a depletion region, where the charge carriers "cancel", leaving the high resistivity of the bulk crystalline in a small region
    - Applying a reverse bias tries to push electrons from the N-type material into the P-type, expanding the depletion region and causing no current to pass through due to the high resistance
    - Applying a forward bias does the opposite and shrinks the depletion region
        * With a smaller voltage the region shrinks but still exists, causing some but not a lot of current to flow
        * After reaching a critical voltage, the depletion region is fully eliminated and now resistance is low and potentially large currents can pass
- For an ideal diode, we have two regions: in the reverse bias region $V < 0$, the diode becomes an open circuit and $I = 0$; in forward bias $I > 0$, so $V = 0$ and we model the diode as a closed circuit
    - Using a diode with an op-amp circuit creates an output that is similar to ideal
    - This model is suitable for low-fidelity, quick analyses because it can produce ambiguous results
    - Note the problem here is that we can't really define where the diode switches between the two states, since $V = 0$ when the diode is a closed circuit
        * This means that to use the model, we need to first take a guess at the voltage bias on the

diode, solve the circuit, and then confirm that our guess was correct
    * If we assume reverse bias, and find a positive voltage on the diode, we need to flip it
    * If we assume forward bias, and find a negative current across the diode, we need to flip it

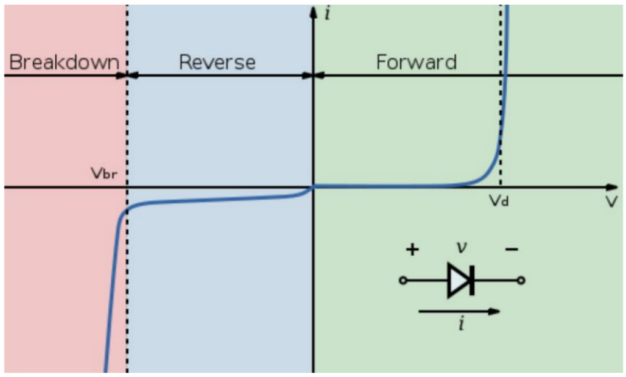

Figure 27: Real-world diode characteristic curve.

- In reality the behaviour of the diode looks more like the graph above
- Improved model 1: constant voltage model
  - Under some fixed voltage V_{D_0}, we model the diode as an open circuit
  - Above this fixed voltage, the diode acts as a closed circuit but with a voltage drop
  - We model it as a constant voltage source of voltage V_{D_0} to represent the constant voltage drop across the diode when it's conducting
    * Note this is not a true voltage source because it cannot deliver current!
  - 0.6 to 0.7V is a typical voltage drop for a silicon diode
  - As with the ideal model, we can start by assuming reverse bias, then checking if the diode has a voltage greater than V_{D_0}; if it is, then we assume forward bias and solve the circuit again
  - With this model, we can also calculate the power dissipation as $P = IV_{D_0}$
- Improved model 2: piecewise-linear model
  - Use an added series resistance to model the change in V vs. I in forward bias
  - In forward bias, we replace the diode with both a voltage drop of V_{D_0} and a series resistance r_D
    * The condition for forward bias is now $V > V_{D_0}$
    * With this model, we no longer have an ambiguity in the condition check since the same variable is used for both forward and reverse checks
  - This has better fidelity, but r_D needs to be fitted to real life conditions
    * The value of r_D can change for low vs. high currents, so if we fit it in one range it will be increasingly less accurate in the other
  - This model is good for a quick analysis of the current and power dissipation through the diode
- Improved model 3: exponential model
  - This model is more accurate but not suitable for hand calculation
  - Forward bias is modelled as $I_D = I_S \left(e^{\frac{V_D}{nV_T}} - 1 \right)$
  - Reverse bias is modelled as a constant small reverse current $I_D = -I_S$, so that we avoid ambiguity when checking later
  - The parameters come from the underlying physics:
    * I_S: saturation current, on the order of 1×10^{-12} A to 1×10^{-15} A; this is the current that flows through the bulk crystalline structure (diffusion of minority carriers)
    * V_T: thermal voltage, usually 25mV at room temperature; this models the thermal response of the diode
      - Sometimes diodes can heat up, which causes them to pass more current, which in turn causes them heat up even more in a positive feedback loop
    * n: ideality factor, typically 1-2; this accounts for inaccuracies in our model
  - This model has near-perfect fidelity, but is not suitable for hand calculation

  - Procedure:
    1. Assume some initial guess for I_D using the constant voltage model
    2. Calculate the diode voltage from I_D by reversing the model
    3. Treat the diode as a constant voltage drop we just calculated, and find the current through the diode by solving the rest of the circuit
    4. Repeat the previous steps until the change to the diode current between iterations is small, which indicates that we've reached a sufficient degree of precision
  - We could also start with a voltage guess and iterate based on that, but since the model is much less sensitive to current, having a bad current guess is much better than having a bad voltage guess
- If a sufficiently large reverse voltage is applied, the diode can break down
  - The large electric field creates additional temporary charge carriers, causing an avalanche effect; substantial reverse current can flow in breakdown
  - This effect is not permanent and can be reversed if the voltage/current drops
  - Most of the time this is undesirable; it's hard to take advantage of because the breakdown voltage is hard to predict
- The transition between forward and reverse modes takes a nonzero amount of time, during which current can flow in the wrong direction
  - The *reverse recovery time* T_{rr} is the time required for the transition
  - During T_{rr}, even though the voltage should put the diode into reverse bias, it will keep conducting
  - This can lead to destructing of the diode
  - Some diodes are faster; a typical diode recovers in about 1ms, with special diodes (e.g. Schottky) bringing this down to 10ns or less
  - However there is a tradeoff between the reverse recovery time and other design parameters

Lecture 12, Oct 18, 2023

Regulator Circuits

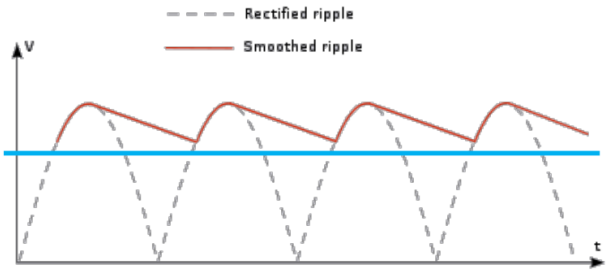

Figure 28: Voltage regulator input vs. output.

- The goal of a regulator is to produce a constant DC output voltage (generally from a higher input voltage) which is constant and steady under load variation
- A regulator is often attached to the output of an AC rectification circuit, which is noisy and contains ripples
- We want the output of our regulator to look like the blue plot above, even if the input voltage varies or if the output load draws varying amounts of current
- Two properties of regulators are of interest:
  - *Line regulation*: holding output constant while input voltage changes
    * This is usually analyzed under the worst-case load current scenario
    * For simple regulators, the highest load current is typically the worst-case scenario; for more complex regulators this can be the lowest load current
    * This is generally quantified as the difference between V_{OUT} at maximum V_{IN} and V_{OUT} at minimum V_{IN} (both at the worst load current), normalized by the design V_{OUT} (nominal value)

        - Note sometimes the V_{OUT} at max or min input voltage are used as normalization for more complex circuits
    * Line regulation is often expressed as a percentage, which would be the percent change in V_{OUT} for every 1% change in V_{IN}
        - Single digit values are good, double digit values are generally poor
  - *Load regulation*: holding output constant while load current changes
    * For simple regulators, the lowest input voltage is typically the worst-case scenario
    * This is generally quantified as the difference between V_{OUT} at minimum load and V_{OUT} at maximum load (both at the worst input voltage), normalized at the V_{OUT} at maximum load
        - Note we are doing min minus max, because generally with a higher load we expect the output voltage to go down
        - Some manufacturers will normalized by V_{OUT} at minimum load or nominal V_{OUT}
  - Load and line regulation are signed quantities, but they are typically positive unless there is feedback in the circuit
- For most simple (no active feedback) regulator circuits, the ends of the input/current draw ranges are usually where the regulator behaves the poorest
- Most regulator circuits take advantage of the fact that the voltage drop across a diode in forward bias is nearly constant
  - Typically if a regulator circuit is working, diodes will be in forward bias mode
- Let's try to design a regulator with the following requirements:
  - Input voltage varies from 10-15V
  - Load current varies from 0-1A
  - Desired output is 9V

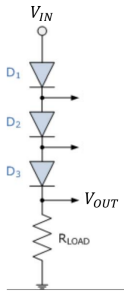

Figure 29: Series diode regulator.

- Example: series diode regulator
  - R_{LOAD} is a placeholder load which can draw varying amounts of current as specified above
  - We will be using the piecewise-linear model with $V_{D_0} = 0.5\,\text{V}$ and $r_D = 0.1\,\Omega$
  - On a high level we expect the output to be a constant voltage offset from the input due to the series diodes
  - This regulator has poor line regulation, but good load regulation
  - To find line regulation, we solve the circuit for $V_{IN} = 10\,\text{V}$ to $15\,\text{V}$; in both cases we solve with $I_{LOAD} = 1\,\text{A}$ since it is our worst-case scenario
    * Assuming forward bias on all diodes, we have 3 resistors r_D in series and 3 voltage sources V_{D_0} in series
    * Note generally when diodes are in series with no connections in-between, they will always have the same state
    * At $V_{IN} = 10\,\text{V}, I_{LOAD} = 1\,\text{A}$ each r_D has a voltage drop of $0.1\,\text{V}$ and each V_{D_0} has a voltage drop of $0.5\,\text{V}$, resulting in $8.2\,\text{V}$
    * At $V_{IN} = 15\,\text{V}$, the analysis is similar and we get $13.2\,\text{V}$
    * The line regulation is then $\dfrac{13.2 - 8.2}{9} = 55.6\%$, which is very bad
    * Note for this circuit, it doesn't matter what load current we chose

- To find load regulation, we solve the circuit for $I_{LOAD} = 0\,\text{A}$ to $I_{LOAD} = 1\,\text{A}$
  * First assume $V_{IN} = 10\,\text{V}$, then at $I_{LOAD} = 0\,\text{A}$ we have $8.5\,\text{V}$ and at $I_{LOAD} = 1\,\text{A}$ we have $8.2\,\text{V}$
    - The load regulation is $\dfrac{8.5 - 8.2}{8.2} = 3.7\%$ which is pretty good
  * If we solve at $V_{IN} = 15\,\text{V}$, we get $13.5\,\text{V}$ at no load and $13.2\,\text{V}$ at maximum load
    - The load regulation is $\dfrac{13.5 - 13.2}{13.2} = 2.3\%$, which is better than the minimum input voltage case
    - This confirms that the minimum input voltage is the worst case

Lecture 13, Oct 20, 2023

Diode Shunt Regulator

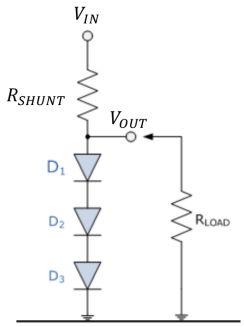

Figure 30: Diode shunt regulator circuit.

- The idea is that we're shunting the current that the load is not using through the diodes
- We expect this to have good line regulation since here V_{out} is essentially equal to the constant voltage drop across all the diodes
  - We can also design it for good load regulation
- Our operating condition are the same as the previous example:
  - Input voltage from 10-15V
  - Load current from 0-1A
  - Desired output is 9V
- We will modify the circuit to have 15 diodes in series instead of 3, all with a piecewise linear model; we will use a shut resistance of $R_{SHUNT} = 3.5\,\Omega$
- Since the diodes are all in series, they will share the same state, which we assume to be forward bias
  - Each diode is replaced with a constant voltage drop of $0.5\,\text{V}$ and a series resistance of $0.1\,\Omega$
  - This leads to a total voltage drop of $7.5\,\text{V}$ and resistance of $1.5\,\Omega$
- Line regulation: test two cases, $V_{IN} = 10\,\text{V}$ and $V_{IN} = 15\,\text{V}$, under a load current of $I_{LOAD} = 0\,\text{A}$
  - In this case the worst-case scenario is reached when the diodes are on the edge of being in reverse bias; this generally happens when we don't pull enough current or pull too much, but it is the former case that is more common
  - Node equation at output: $\dfrac{V_{OUT} - V_{IN}}{R_{SHUNT}} + I_LOAD + \dfrac{V_{OUT} - 7.5}{1.5} = 0$
  - At $V_{IN} = 10\,\text{V}, V_{OUT} = 8.25\,\text{V}$
  - At $V_{IN} = 15\,\text{V}, V_{OUT} = 9.75\,\text{V}$
  - The line regulation is $\dfrac{9.75 - 8.25}{9} = 16.7\%$, which is okay (but not very good)
    * The problem is that the design point for the circuit is different – the value of R_{SHUNT} is selected so that we can deliver larger currents; if we had chosen a larger resistance and limited our current range, we will see much better performance
- Load regulation: test two cases, $I_{LOAD} = 0\,\text{A}$ and $I_{LOAD} = 1\,\text{A}$, under an input voltage of $V_{IN} = 10\,\text{V}$

  - For pretty much all regulators without feedback, the worst case occurs with minimum input voltage; at minimum input voltage we're the most susceptible to losing forward bias on the diodes
    * This is referred to as the "dropout voltage", which is the minimum difference between V_{OUT} and V_{IN}
  - At $I_{LOAD} = 0\,\text{A}, V_{OUT} = 8.25\,\text{V}$
  - At $I_{LOAD} = 1\,\text{A}, V_{OUT} = 6.5\,\text{V}$
    * Note if we had assumed that the diodes are all in forward bias, we would have found $V_{OUT} = 7.25\,\text{V}$; this would mean less than 0.5 V per diode, so we lose forward bias
    * In reverse bias we simply have $V_{OUT} = V_{IN} - R_{SHUNT} I_{LOAD} = 6.5\,\text{V}$
  - The load regulation is $\dfrac{8.25 - 6.5}{6.5} = 26.9\%$ which is quite bad
- This is a pretty good voltage regulator if we make sure that it does not drop out, so for higher current outputs we need to make sure that the input voltage stays high
- Note that in practice the power consumption of this circuit is quite high

Zener Diodes

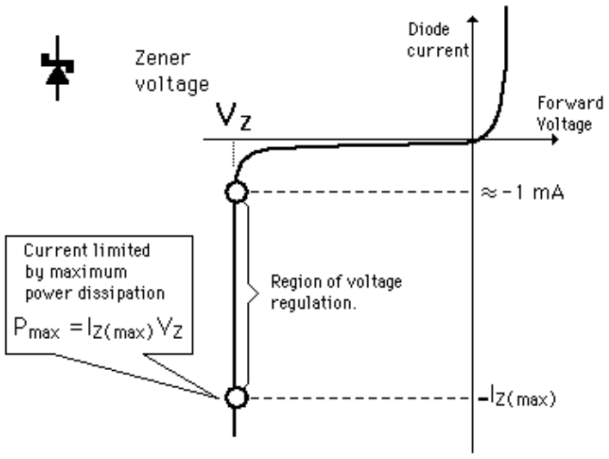

Figure 31: Model of a Zener diode.

- A zener diode is a diode engineered to undergo reverse breakdown non-destructively at a specific voltage
  - In forward bias it behaves similar to a regular diode, but in reverse we're able to get a very specific breakdown voltage that can be quite large
  - Typically zener diodes are used in reverse bias in its zener region
- Most often zener diodes are analyzed using a piecewise linear model; we will use a constant voltage model
  - We can replace a zener diode with just a constant voltage source, provided the reverse voltage is high enough
  - Note that because most diodes have a low voltage dissipation, for a larger zener voltage we will have very low current ratings
  - We neglect the linear resistance since most of the time we will have low current
- Example: for the zener shunting regulator above, select the zener voltage V_Z and R_{SHUNT} and determine the current range it operates in; assume $V_{OUT} = 10\,\text{V}$ and V_{IN} is in the range of 12-18V, and the zener diode can dissipate 0.5W of power
  - If we use a constant voltage model we immediately see that $V_{OUT} = V_Z$, so we can select the zener voltage as 10V immediately
  - The worst-case scenario for the input voltage is $V_{IN} = 18\,\text{V}$, which will give the highest current draw
    * Higher V_{IN} pushes more current through the shunt, which in the worst case will all go through

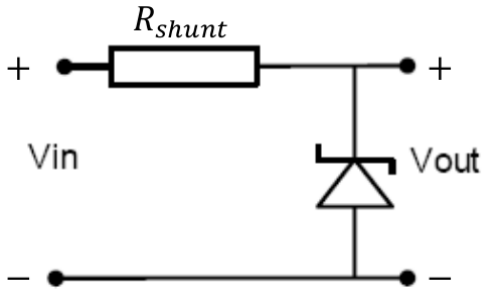

Figure 32: Example problem.

the diode

* Under this scenario and assuming $I_{LOAD} = 0\,\text{A}$ the diode dissipates a power of $V_{OUT}\dfrac{18 - V_{OUT}}{R_{SHUNT}} = 0.5\,\text{W}$, which we can solve to get $R_{SHUNT} = 160\,\Omega$
* Note we always want to make R_{SHUNT} smaller because this limits the maximum amount of current we can draw

– To see how much current we can draw, we need to consider the worst case V_{IN}

* The critical point is when $\dfrac{V_{IN} - V_{OUT}}{R_{SHUNT}} \leq V_Z$ which is when the diode drops out
* We also need $I_D \geq 0$ and $I_D = \dfrac{V_{IN} - V_Z}{R_{SHUNT}} - I_{LOAD}$; so when $V_{IN} = 12\,\text{V}$ and $I_D = 0$ we get a current limit of 12.5 mA (which is higher for a higher V_{IN})

- Zener voltage references are the standard if we want to produce a precise voltage at a low current

Rectifier Circuits

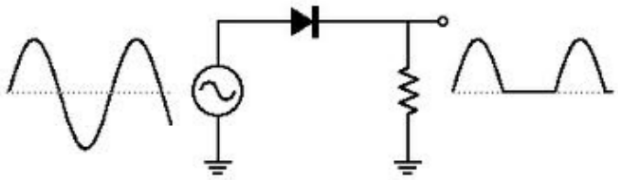

Figure 33: Example half-wave rectifier.

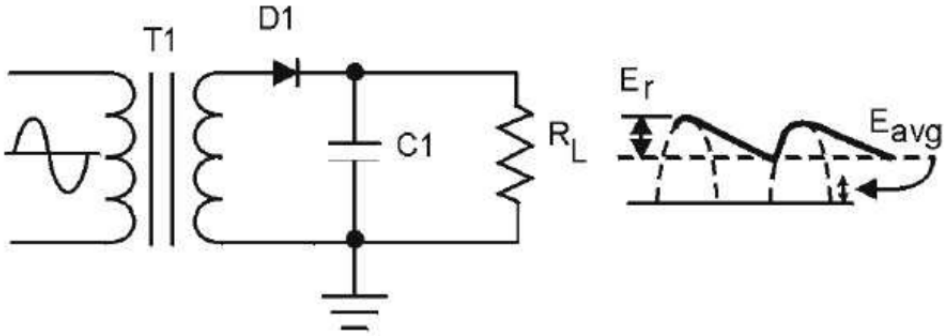

Figure 34: Half-way rectifier with capacitor.

- A rectifier circuit converts an input AC voltage into an output DC voltage

- In the example half-wave rectifier above, the diode will allow current to pass through whenever the AC voltage is positive, and block it when the voltage is negative
  - However this is produces an output that is far from DC since whenever the AC voltage goes negative, our DC voltage goes to zero
- To counteract this we use components that can store energy – capacitors and inductors; this will give us a wavelike output, which we can describe as DC plus some *ripple*
  - The amount of ripple is proportional to the current drawn and inversely proportional to the capacitance
  - Note that this puts a large reverse voltage on the diode, so we need to select the diode accordingly
  - If we attach a capacitor however, we get a large current spike when both the load and capacitor are getting current; therefore we need to make sure that the peak current rating for the diode is high enough
    * This also increases the reverse voltage; in the worst case, we can see up to twice the original value

Lecture 14, Oct 25, 2023

Regulator Design

- Diode selection is made more complex in a rectifier with a capacitor:
  - Input current only flows for a short period of time each cycle, which charges the capacitor and supplies the load – this leads to a significant current spike, so we need to ensure the peak repetitive surge current of the diode is high enough
  - Peak reverse voltage across the diode also increases significantly, since the output voltage stays high while the input voltage drops negative – the voltage drop is now close to twice the peak voltage minus the diode drop
    * Smaller ripple makes the peak reverse voltage closer to this
    * $PIV = 2V_p - V_{D_0}$
- The high peak current draw is a problem for power distribution grids, so we usually use some form of *power factor correction* to account for this
  - We can put an inductor in series with the input current; since the inductor resists change in current, this smoothes out the peaks (in theory, while in practice this doesn't work too well)

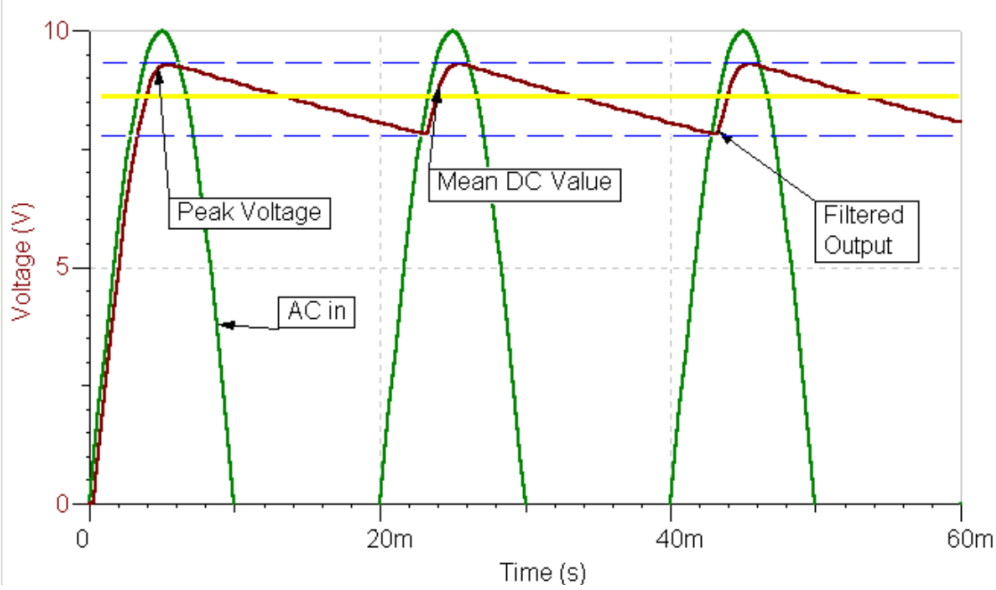

Figure 35: Plot of the output from a rectifier.

- The ripple voltage V_{RIPPLE} is typically defined as the peak-to-peak voltage difference of the output (distance between the two blue lines)
- For a capacitor, $V_{RIPPLE} = \frac{I_{LOAD}}{fC}$
  - Here we assume that the load current is roughly constant, which makes a straight-line approximation of the capacitor discharge valid
  - A larger capacitor and higher frequency (so peaks are closer) reduce the amount of ripple
- Note that in rectifier circuits, we typically use a *transformer*, which is a pair of coupled inductors wrapped around the same core; this steps down the line voltage and adds isolation between our circuit and the input
  - If the input (*primary*) winding is N_P and the output (*secondary*) winding is N_S, then the output voltage is $V_S = V_P \frac{N_S}{N_P}$
- Sometimes we will use the RMS voltage of the input AC signal, which can be converted into peak voltage by multiplying by $\sqrt{2}$

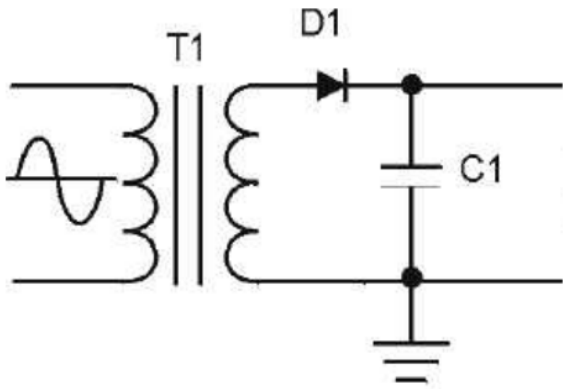

Figure 36: Example problem.

- Example: design the above half-wave rectifier by selecting C_1 and the RMS secondary voltage required for T_1, and specify the minimum PIV for D_1; the power supply will be regulated by a circuit that outputs 5 V DC and requires an input of at least 7 V; we want 20 mV peak-to-peak ripple, given a maximum load current of 1 A and $f = 60$ Hz; assume $V_{D_0} = 1.0\,\text{V}, I_D = 1\,\text{A}$
  - Note that typically instead of targeting a small ripple input to the regulator, we typically leave the ripple rejection to the regulator
  - We can use the formula to solve for C_1 from the amount of ripple; we get $C \geq 0.833\,\text{F}$ (which is quite unrealistic)
  - Adding the ripple to the minimum output voltage and adding the capacitor voltage drop gets us a secondary voltage of about 8 V (where we have ignored the ripple voltage since it is comparatively small), or 5.66 V RMS
  - Therefore the PIV can be calculated by taking twice the peak secondary voltage and subtracting the diode drop, which is 15 V

Full-Wave Rectifiers

- By using a full-wave rectifier, we can effectively double the number of charging cycles (the input frequency), allowing us to select a smaller capacitor and get less ripple
- One way of implementing this is using a *center-tapped winding* on the transformer; this behaves like two separate secondary windings connected in series, so if we connect the center to ground, we get essentially a positive and a negative version of the AC signal
- These two signals are then fed through diodes and into the same capacitor circuit to rectify

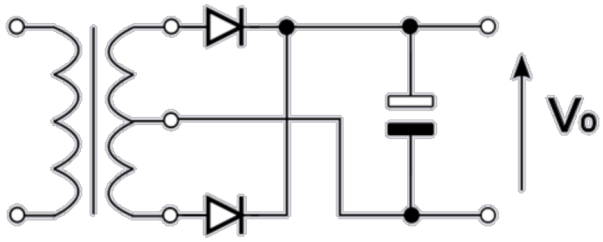

Figure 37: Full-wave rectifier circuit.

Lecture 15, Oct 27, 2023

Full-Wave Rectifier Example

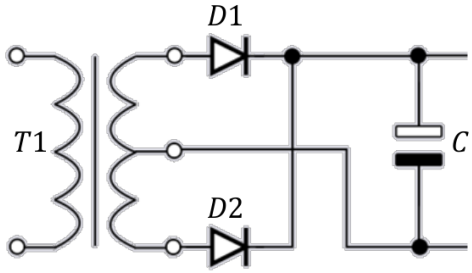

Figure 38: Example problem.

- Example: design the circuit above by selecting C_1 and the RMS center-tapped secondary voltage for the transformer T_1 and determining the PIV required for the diodes; the power supply is regulated by a regulator that outputs $10V$, requiring a voltage of at least 12 V and has 40 dB of ripple rejection; we want the overall output of the power supply to have 20 mV ripple given a max load of 1 A and $f = 60$ Hz; assume $V_{D_0} = 1.0$ V at $I_D = 1$ A
  - A ripple rejection means that the input ripple to the regulator will be reduced by a factor of 40 dB, i.e. divided by 100
  - This means we can tolerate up to 2 V p-p of ripple from the rectifier
  - We need the peak voltage minus the diode drop minus the ripple to stay above 12 V
    - $\frac{V_{SEC_p}}{2} = 12 + 2 + 1 = 15$ V
    - Multiply by 2 to get the peak-to-peak voltage of the secondary, and convert to RMS
    - $V_{SEC_{p-p}} = 21.2$ V (RMS, CT)
  - $V_{R_{p-p}} = 2 = \frac{I_{LOAD}}{2fC} \implies C = 4170\,\mu\text{F}$
    - Note that we'll get 2 peaks for every full cycle of the AC, so in effect by using a full-wave rectifier we have doubled the frequency
    - Sometimes we need to pick the capacitor's working voltage, which we can determine by checking the maximum voltage, in this case 14 V $(12 + 2)$
    - This will be an electrolytic capacitor
  - Note that our peak inverse voltage doesn't change compared to the half wave rectifier case; it's still $PIV = 2V_{IN_p} - V_{D_0} = 29$ V
    - The peak input voltage is half of the secondary peak to peak voltage
- Typically a more efficient rectifier will increase the frequency of the input AC to achieve smaller capacitance requirements

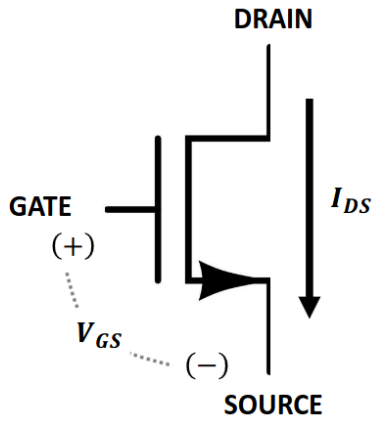

Figure 39: A MOSFET.

Transistors and MOSFETs

- MOSFET stands for Metal Oxide Semiconductor Field Effect Transistor
- Transistors are active, three-terminal devices that provide a path for (potentially large) currents to flow, along with an input control
- For a MOSFET, the control signal is called the *gate*, while the input and output for the current are the *drain* and *source
  - V_{GS} is defined as the relative voltage between gate and source
  - Applying some V_{GS} will cause current I_{DS} between drain and source; just like a diode, under normal circumstances drain to source is the only direction that current can flow
    * This is a *transconductance amplifier*, since a (possibly small) voltage input controls (a possibly large) a current output
- In general we have 3 different states for the MOSFET where two are conducting states; one of these states is associated with switching applications (on/off), another one is associated with amplification

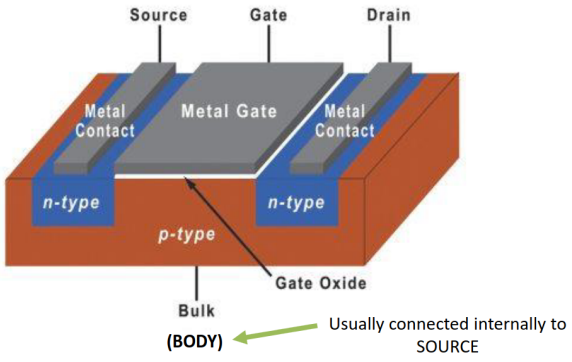

Figure 40: Structure of a MOSFET.

- A MOSFET has the following structure:
  - The bulk material is made of p-type semiconductor
  - Two cavities are made where n-type semiconductor is filled in; one is connected to the source, one is the drain
  - A gate oxide layer acts as insulation between the metal gate and the body
  - Where the two meet, we have a depletion zone where current cannot conduct – this gives us a default state of high resistance
  - Right now we have 4 terminals; to get this to a regular transistor we short the body and source

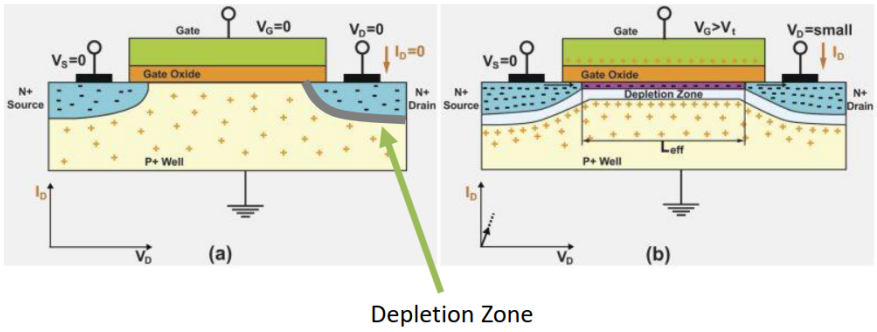

Figure 41: Physics of the MOSFET.

- The MOSFET is made active by applying a potential to the gate
  - If the gate has a potential relative to the body, the charge carriers in the p-type body is separated and drawn to the surface
  - This knocks off a little bit of the depletion zone, so we get a continuous path (channel) between drain and source
  - This can be accomplished with depletion-mode or enhancement-mode
- Like a diode, in order to form the channel, we need a minimum threshold voltage V_T which V_{GS} must reach, below which the MOSFET remains in cut-off
  - Usually in the order of a few volts
  - Note this doesn't yet tell us about how much current can flow or how much we can control the current

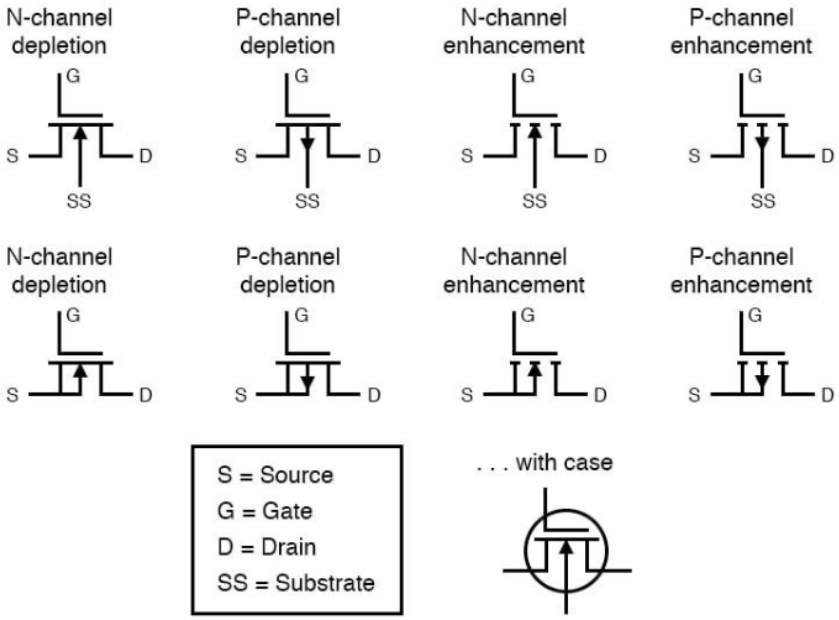

Figure 42: MOSFET symbols.

- Note that there are many different MOSFET symbols, all made to reflect the actual construction of the MOSFET; however they don't really change the math much, so we will use the simplified symbol (first image in this section)
  - The separation between the gate and the source/drain implies that at least at DC, current cannot flow into the gate

- Once the channel is created, current can flow with varying resistance from drain to source; there are 2 modes:
  - *Triode mode*: unrestricted channel, small drain to source voltage/resistance
    * This is the "switching" mode
    * Low power is dissipated because we have low resistance, so the switching is efficient
    * We can use this as a switch to control a larger current with a small voltage
      - However we don't get any control over how much current passes through even as we vary V_{GS}
    * This requires $V_{GS} > V_T$ and V from drain to source is small
    * Typically we set up $V_{GS} \gg V_T$ because the larger our gate voltage, the more current we can pass through with the MOSFET still remaining in triode mode
  - *Saturation mode*: restricted channel with *pinch-off*
    * This requires $V_{GS} > V_T$ but $V_{GS} \approx V_T$
    * Now we have V_{DS} being potentially large
    * The degree of pinch-off varies proportionally with V_{GS}, so the output current flow is proportional to the input voltage
    * In this mode, we have a transconductance amplifier

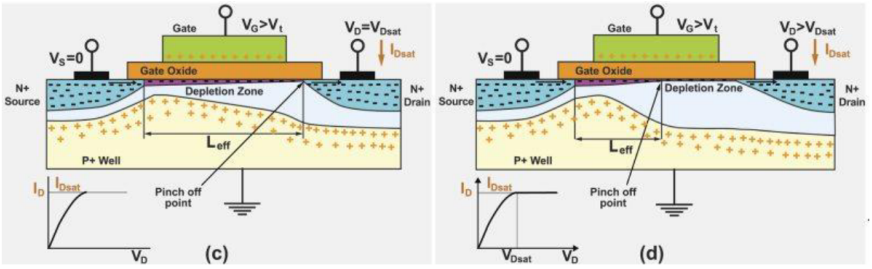

Figure 43: MOSFET in saturation mode.

- When $V_{GS} < V_T$, the MOSFET is always in cut-off mode with no current flowing anywhere, so we model the MOSFET as an open circuit
- When $V_{GS} \geq V_T$, the MOSFET is in one of two conducting modes
  - The triode mode is modelled as a fixed, low-value resistance $r_{DS_{ON}}$
    * The current is not really dependent on V_{GS}
  - The saturation mode is modelled as a current source that is a direct function of input voltage, $I_{DS} = f(V_{GS})$
    * This much current flows pretty much regardless of what is attached to the terminals
  - Note that the exact boundary between the two modes is dependent on the applied voltage
    * $V_{DS} = V_{GS} - V_T$ is the exact boundary between the two modes
  - We can also have devices on the boundary between two modes
    * On the boundary, both sets of mode equations apply

- The exact formula for triode mode is $I_{DS} = \dfrac{k_n' W}{L}\left((V_{GS} - V_T)V_{DS} - \dfrac{1}{2}V_{DS}^2\right)$
  - This requires $V_{GS} \geq V_T$ and $V_{DS} \leq V_{GS} - V_T$
  - But typically V_{DS} is very small so the second term can be ignored, giving us a linear approximation
    * Note that this approximation relies on $V_{GS} \gg V_T$, so we typically design to this
  - Therefore we have $I_{DS} \approx \dfrac{k_n' W}{L}(V_{GS} - V_T)V_{DS}$
    * This gives us an equivalent resistance of $\dfrac{1}{\frac{k_n' W}{L}(V_{GS} - V_T)} = r_{DS_{ON}}$
    * Note that this does depend on $V_{GS} - V_T$ but the dependence is relatively small
  - We don't typically calculate this ourselves; rather the datasheet gives this value, usually at a fixed large value of V_{GS}

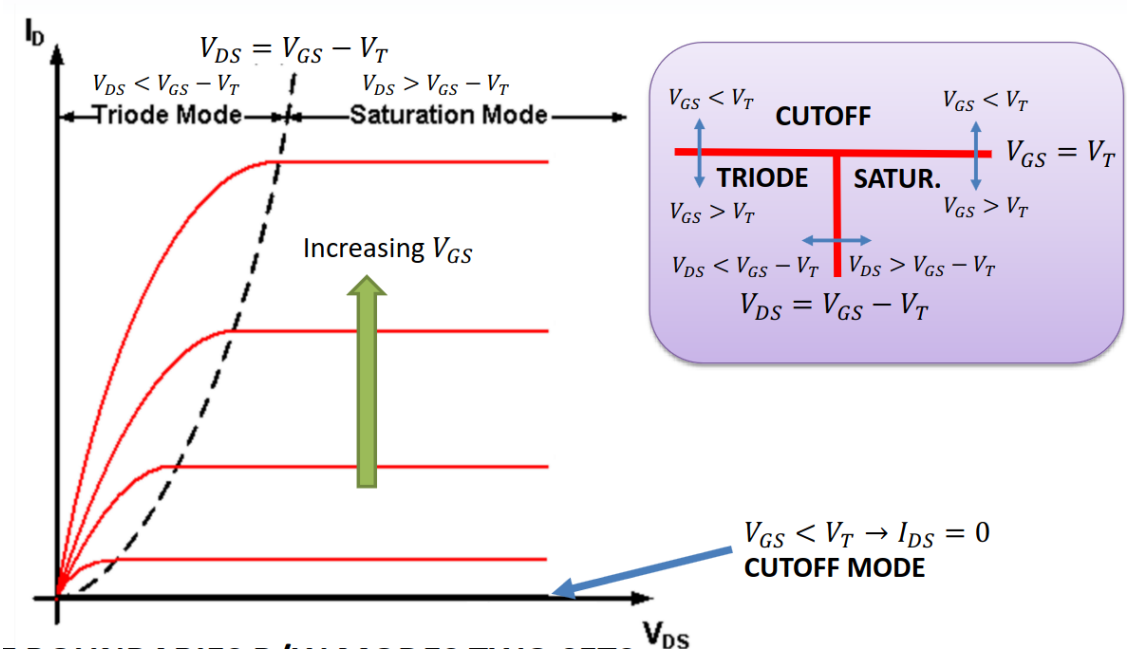

Figure 44: Plot of MOSFET current against drain-to-source voltage.

  - But note that this means we're fitting it to a specific V_{GS} (typically the more vertical bits to the left), so if we're operating close to the boundary we will get wrong results
    * $\frac{k_n' W}{L}$ also depends on the gate voltage so we can't simply use the formula
- In saturation mode, the output current has effectively no dependence on V_{DS}, so I_{DS} is a function of V_{GS} only; however this is a nonlinear effect; I_{DS} increases faster the larger V_{GS} gets
  - This gives us model of $I_D = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_T)^2$
  - The model parameters may be known from material properties but are usually fitted to a datasheet
    * These numbers are different from the ones in triode mode!
  - Nonlinear amplification is bad because it introduces distortion to our signal (BJTs do much better in this aspect)
  - To fix the nonlinearity, we will limit the range of V_{GS} to a small delta around the central value (*operating point*); now we can linearly approximate the result
    * This is called a *small signal model*

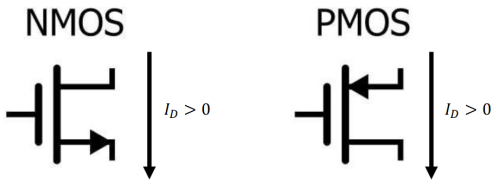

Figure 45: NMOS and PMOS symbol differences.

- Note that so far we've been talking about an N-type MOSFET (NMOS), since it has N-type doping for the source and drain; if we flipped the regions, we get a P-type MOSFET (PMOS)
  - The main difference is that the direction of current flips; in a PMOS the current flows from source to drain
  - We also reverse the inequalities in all of our condition checks, but otherwise keep the same models
  - A different value is also used for k_p'

- I_D is taken as positive but positive I_D is I_{SD} (source-to-drain) instead of I_{DS}
- For a PMOS V_{GS} is typically negative in triode/saturation, and V_T is also negative

Lecture 16, Nov 1, 2023

MOSFET Real-World Issues

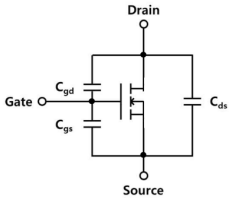

Figure 46: Model of parasitic capacitance in a MOSFET.

- In real life the construction of the MOSFET introduces a parasitic capacitance from gate to source (there are also gate-to-drain, drain-to-source parasitic capacitances but these are small)
  - Typically $C_{GS} \sim 5\,\text{pF} - 50\,\text{nF}$
  - This introduces a time limit for switching since we need to charge the capacitor
  - This can also draw large transient currents when V_{GS} changes rapidly, so we will need a driver IC or series gate resistors to mitigate this issue

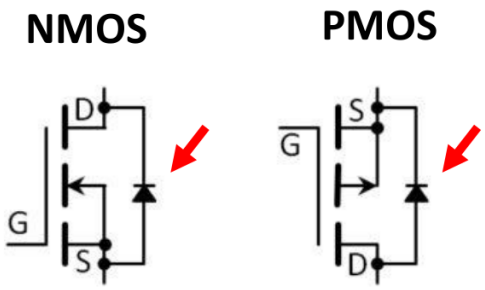

Figure 47: MOSFET body diode.

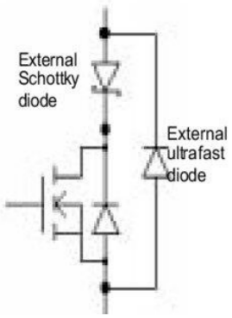

Figure 48: Fixing the MOSFET body diode.

- The construction creates 2 unintended PN junctions between the body and source/drain, which acts as a diode
  - Since we short body to source, one of these will be shorted out; however, the body-drain diode (known as the *body diode*) will now exist between the source and drain

- If the drain-to-source voltage is too large, this diode will enter reverse breakdown and cause issues; this limits the max allowable V_{DS} in all modes
- This diode can also make the MOSFET conduct even when it is in cut-off; this happens when $I_D < 0$
- Sometimes we want a diode in this location (e.g. motor driver) but this is a really bad diode
- Generally we place external diodes with better specifications to fix the problem

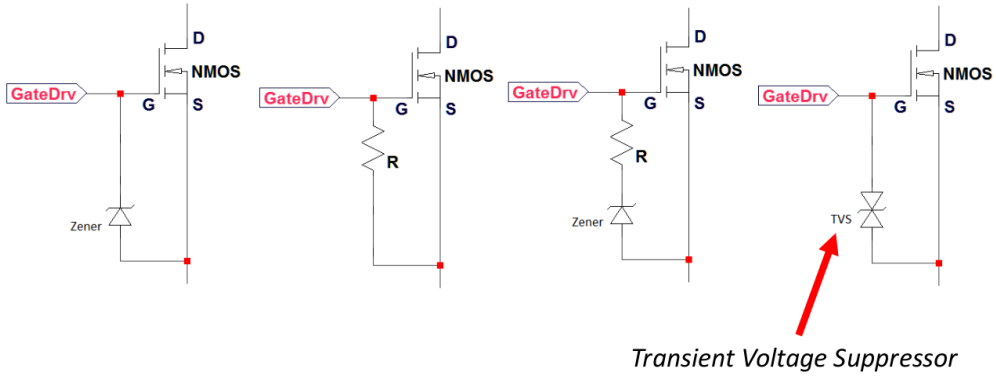

Figure 49: MOSFET ESD protection.

- The thin oxide layer under the gate is very easy to damage; typically V_{GS} is limited to $\pm 10\,\text{V}$ or $\pm 20\,\text{V}$
  - This means static discharge can easily damage the oxide layer
  - Most modern ICs and devices with MOSFETs now have additional ESD protection for this reason

Design Examples

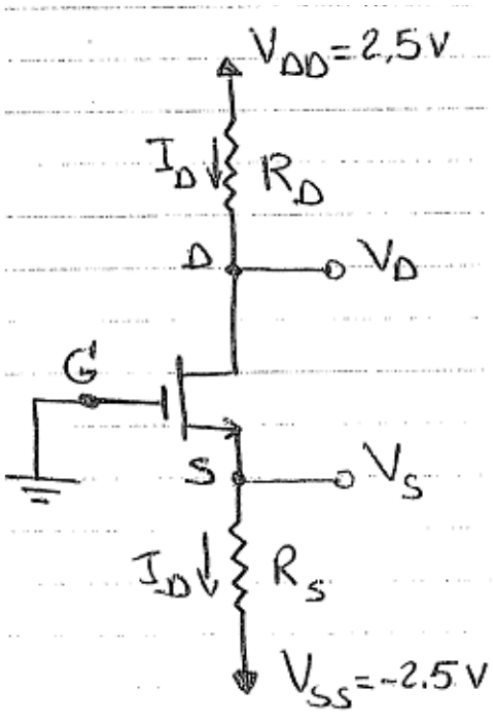

Figure 50: Example circuit.

- Example: design the circuit above for a drain current of 1 mA and a drain voltage of 0 V; the transistor has $V_T = 1\,\text{V}$, $k_n' = 60\,\mu\text{A/V}^2$, $L = 3\,\mu\text{m}, W = 100\,\mu\text{m}$
  - We assume that gate current is 0 at DC, so current into the drain must be the same as current out of the source
    * Therefore generally we use drain current, source current, and drain-to-source current interchangeably
  - Note we always use uppercase subscripts for DC and lowercase subscripts for small signals
  - We usually start at the drain-to-source path
  - Since the voltage at V_D is 0, we know the voltage and current across the resistor R_D immediately
    * $R_D = \dfrac{V_{DD} - V_D}{R_D} = 2.5\,\text{k}\Omega$
  - Now we need to relate V_S to V_D by determining the mode of operation for the MOSFET
    * We will assume one of the conduction modes (since we have a nonzero drain current, it cannot be in cut-off mode)
    * Recall that for saturation, $V_{DS} > V_{GS} - V_T \implies V_D - V_S \geq V_G - V_S - V_T \implies V_D \geq V_G - V_T \implies V_D - V_G > V_T \implies V_{GD} < V_T$
      - This is satisfied in our example
    * Note that in general, we won't always be able to determine the MOSFET's mode of operation directly like this
    * However in general in saturation mode, we typically expect drain to source currents on the order of milliamps or drain/source resistances on the order of kilohms
  - In saturation current is a direct function of V_{GS} so we can find V_{GS} using the MOSFET parameters and find V_S given V_G
    * This will yield us two values 0 V or 2 V, but we can eliminate one since we require $V_{GS} > V_T$
    * At this point we can check our assumption of saturation mode
  - This gives us $V_S = V_G - V_{GS} = -2\,\text{V}$
  - Now we can solve for $R_S = \dfrac{V_S - V_{SS}}{I_D} = 500\,\Omega$
    * Typically in many designs the source resistance is the smaller of the two
- Example: find the drain and source voltage of the MOSFET above, and select a resistor to replace the current source with, without changing the source or drain current
  - We expect the MOSFET to be in saturation mode
  - We have $V_G = 0\,\text{V}, I_D = 2\,\text{mA}$
  - The drain voltage can be calculated by as $V_D = V_{DD} - R_D I_D = 2\,\text{V}$
    * Note when we solve the equation we will get 2 possible values, but one of them will give us cutoff instead of saturation
  - $V_{GD} = -2\,\text{V} < V_T$ so we are indeed in saturation mode
  - Now use $I_D = \dfrac{1}{2} k_n \dfrac{W}{L} (V_{GS} - V_T)^2$, with $I_D = 2\,\text{mA}$ to solve for $V_{GS} = 4\,\text{V}$
    * Again we will get 2 values, but one of them gives us cutoff
  - So $V_S = V_G - V_{GS} = 4\,\text{V}$
  - We can now solve for an equivalent resistance value that can replace the current source: $I_S = I_D = 2\,\text{mA} = \dfrac{V_S - V_{SS}}{R_S}$ to get $R_S = 3\,\text{k}\Omega$

Lecture 17, Nov 15, 2023

More Design Examples

- Example: feedback biasing: for the MOSFET circuit above, find the drain and source voltage and select a resistor to replace the current source
  - $V_S = 0$
  - $I_D = I_S = 2\,\text{mA}$ still because we assume a gate current of 0 at DC
  - $V_{GD} = 0$ forces us to be in saturation, since $V_{GD} < V_T$

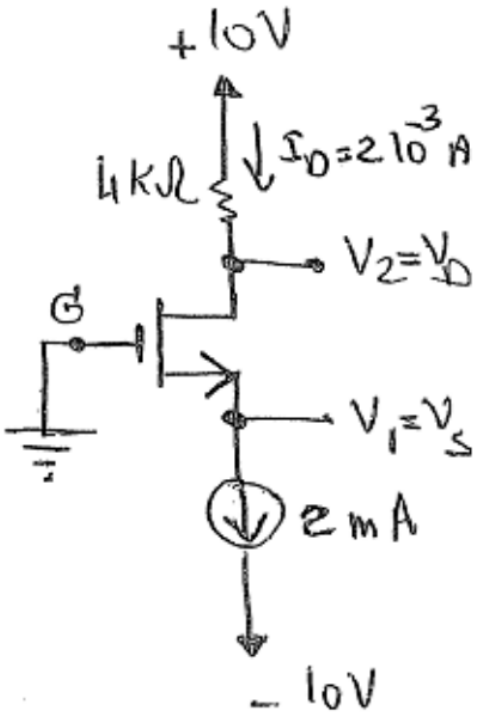

Figure 51: Example circuit.

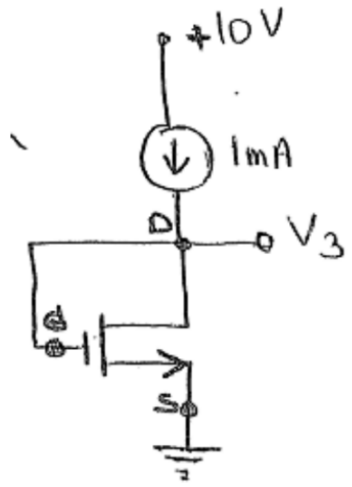

Figure 52: Design example 3.

- $I_D = \frac{1}{2}k_n'\frac{W}{L}(V_{GS} - V_T)^2$, so we can solve for V_{GS} and pick the one that gives us saturation: $V_{GS} = 3.414\,\text{V}$
- $V_G = V_S + V_{GS} = V_D$ to solve for V_{GS}
- With V_{DD} and V_D and the current going through, we can find $1\,\text{mA} = \frac{V_D D - V_D}{R_D} \implies R_D = 6.59\,\text{k}\Omega$
- By itself, this circuit doesn't do much, but we can use it to provide a stable reference current, as a building block in a current source circuit

PMOS Circuits

PMOS Transistor Equations

	Cutoff Mode	Triode Mode	Saturation Mode
Required Condition	$V_{GS} > V_t$	$V_{DS} \geq V_{GS} - V_t$ Or $V_{GD} \leq V_t$	$V_{DS} \leq V_{GS} - V_t$ Or $V_{GD} \geq V_t$
Determined Condition	$I_D = 0$	$I_D = k_p'\left(\frac{W}{L}\right)\left[(V_{GS} - V_t)V_{DS} - \frac{1}{2}V_{DS}^2\right]$	$I_D = \frac{1}{2}k_p'\left(\frac{W}{L}\right)(V_{GS} - V_t)^2$

Figure 53: PMOS transistor equations.

- For a PMOS, we have to flip the equations as above
- Positive current is defined as source to drain
- Note that V_T is negative for a PMOS, but otherwise has the same magnitude

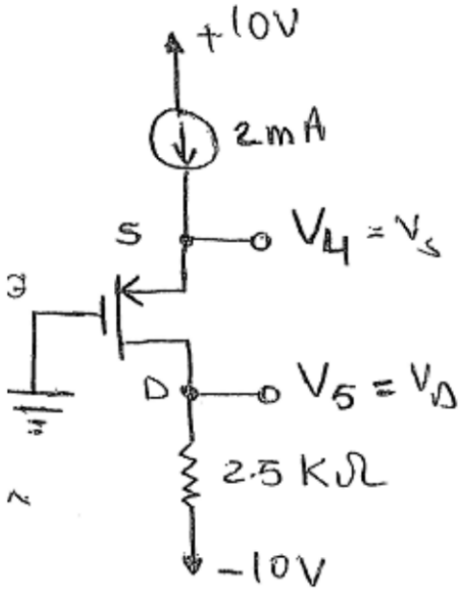

Figure 54: PMOS design example.

- Given $V_T = -2\,\text{V}$, find V_D, V_S, determine an equivalent source resistor; assume $k_p' = 1\,\text{mA/V}^2$
  - We know $I_S = I_D = 2\,\text{mA}$, which already gives us $V_D = V_{SS} + R_D I_D = -5\,\text{V}$
    * Note the "negative supply" is still called V_{SS} even though it's now connected to the drain
  - $V_{GD} = V_G - V_D = 5\,\text{V} > -2\,\text{V} = V_T$, so we have saturation mode
  - $I_D = \frac{1}{2}k_p'\frac{W}{L}(V_{GS} - V_T)^2$ to get $V_{GS} = -4\,\text{V}$ as the voltage that avoids cutoff
  - $V_S = V_G - V_S = 4\,\text{V}$

  - Sanity check: we should normally have $V_S > V_D$ (typically the terminals will be laid out such that the higher voltages are higher on the page)
    * Due to saturation mode, we expect V_S to be quite a bit larger, which is the case
  - This gives $R_S = 3\,\text{k}\Omega$

Lecture 18, Nov 17, 2023

Biasing MOSFET Amplifiers

- To design an amplifier, we have to go through 2 stages:
  - First we set up the circuit to operate at a specific DC configuration
    * This determines the *biasing* of the amplifier
    * This gives us some parameters that determine the amplifier operation – input/output resistance, voltage gain, and indirectly, the voltage limits
  - We will then use capacitors to inject an AC signal and extract the resulting signal
- Note capital letters are generally pure DC, while lowercase letters are AC
- For a single MOSFET there are generally 3 possible amplifier configurations: common source, common drain, and common gate
  - The "common" terminal is the terminal that is not coupled to an input/output
- There are several ways to do biasing:
  - Fixed V_{GS} biasing: fixing V_{GS}, where source and gate are connected to some constant voltage
    * This is the simplest, but least useful because it is very sensitive to V_{GS} and has a small operating range
    * The circuit might have a lot of gain, but it will be very sensitive to tolerances
    * We are essentially overconstraining the problem
  - Fixed V_G biasing: fixing V_G and adding a source resistor
    * An increase in current leads to an increased voltage drop across the resistor, which raises V_S
    * With a fixed V_G, this decreases V_{GS} and decreases the current – this is negative feedback
    * This gives us a much wider range of operation – V_{IN} can be a much larger range and still have good gain
    * Introducing the source resistor reduces the output range, which can be fixed using a capacitor, either replacing or in parallel with the source resistor (*bypass capacitor*)
  - Feedback biasing: connect the drain and gate together, with a gate resistor between them
    * Since no current flows into the gate at DC, the resistor has no impact on the gate resistance, so we just have $V_D = V_G$
    * $V_{DG} = 0$ which makes the MOSFET always in saturation (with some limitations)
  - Constant current source (CCS) biasing: connecting a constant current source at the source to set the DC drain/source current
    * We can add a bypass capacitor from source to ground, so for AC the capacitor grounds the source
    * We can implement the current source using a *current mirror*
- The operating range is restricted due to the modes of the transistors
  - Usually at one end we will get triode mode on some resistors and the other end will give us cutoff mode
  - In both cases we would usually get clipping
- The current mirror shown above behaves equivalently to a constant current source
  - Note the current I_{D_1} is mirrored in I_{D_2}
  - This only works if the MOSFETs stays in saturation; Q_1 is feedback biased, so it will always be in saturation, but note Q_2 does not have this guarantee
    * Q_1 in saturation creates some V_{GS}, which will be copied exactly by Q_2
    * Assuming that Q_2 has the same parameters, we copy the current in Q_1 exactly to Q_2
- Example: design the above circuit so that all transistors operate in saturation, the current source

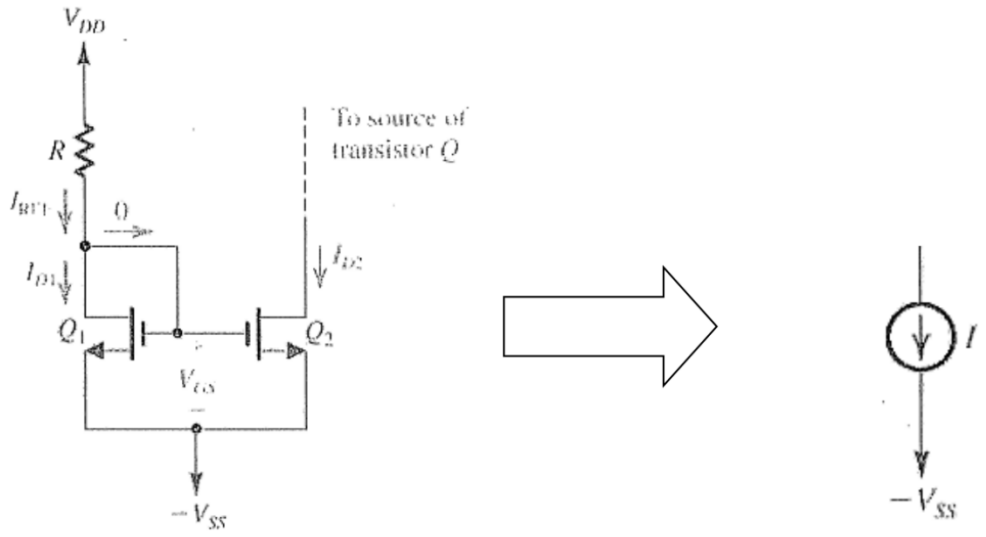

Figure 55: Current mirror circuit.

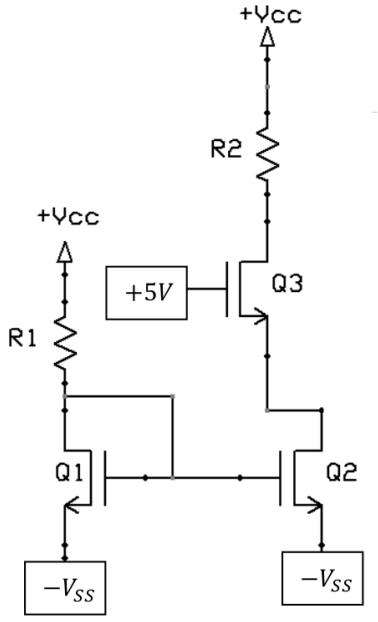

Figure 56: Example circuit using CCS biasing.

provides 2 mA, and the drain of Q_3 has a quiescent (i.e. bias point) of $\frac{V_{CC}}{2}$; assume $V_{DD} = V_{SS} = 15\,\text{V}, k_n' = 4\,\text{mA/V}^2, W = 250\,\mu\text{m}, L = 5\,\mu\text{m}, V_T = 4\,\text{V}$

- We know that Q_3, Q_2 must have $I_D = I_S = 2\,\text{mA}$, and due to the current mirror we want Q_1 to have this as well
- At DC we want the drain voltage to be 7.5 V
- Starting with the current mirror:
  * Q_1 is always in saturation since $V_{DG} = 0$
  * $I_{D_1} = \frac{1}{2}k_n'\frac{W}{L}(V_{GS_1} - V_T)^2 = 2\,\text{mA}$
  * We can now solve for $V_{GS_1} = 4.14\,\text{V}$, discarding the other result of 3.86 V since that gives us cutoff
  * Note that the current in this branch cannot go through any of the gates, so I_{D_1} is also the current through R_1
  * Therefore $V_{D_1} = V_{G_1} = V_{GS_1} - V_{SS} = -10.86\,\text{V}$ and use this to find $R_1 = 12.93\,\text{k}\Omega$
- Note $V_{GS_1} = V_{GS_2}$, so if Q_2 is in saturation, we will also get 2 mA on the right
  * We will solve the circuit with this assumption and then check the mode of Q_2 later
- Given that we know V_{D_3} and $I_{D_3} = I_{D_2}$ we can solve for $R_2 = 3.75\,\text{k}\Omega$
- We've already found all component values, but we need to go back and check our assumptions
  * For Q_3, $V_{DS_3} = V_{D_3} - V_{S_3}$; we need to check if this is greater than $V_{GS_3} - V_T = V_{GS_2} - V_T$ (since all transistors are the same and must give $I_D = 2\,\text{mA}$)
  * Since $V_{GS_3} = V_{GS_2} = 4.14\,\text{V}$, this gives us $V_{S_3} = V_{G_3} - V_{GS_3} = 0.86\,\text{V}$ – use this to check that the inequality is satisfied and Q_3 is in saturation
  * We also have $V_{D_2} = V_{S_3} = 0.86\,\text{V}$, so $V_{DS_2} = 15.86\,\text{V} > V_{GS_2} - V_T = 0.14\,\text{V}$, so Q_2 is also in saturation
- Note the saturation mode equation is an approximation since there are other real world effects; in the real world voltages will be slightly different

Small Signal Amplifiers

- The general idea is that we will couple in an AC signal to our MOSFET circuit using capacitors, which will be amplified
- The DC operating point (biasing) of the amplifier restricts its operating range and also how it behaves as an amplifier – voltage gain, effective resistance, effective source/output resistance
- We will often bias the amplifier to operate "halfway" between the boundaries of cut-off and triode mode

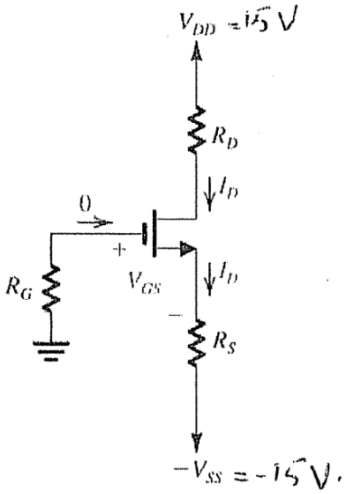

Figure 57: Example.

- Example: design the circuit above so that the MOSFET operates halfway between cut-off and triode mode, with $I_D = 2\,\text{mA}, V_T = 0.8\,\text{V}, k_n' = 50\,\mu\text{A/V}^2, W = 200\,\mu\text{m}, L = 4\,\mu\text{m}$
  - The output will idle at some value and any time-changing signal will vary the output level
  - This output level is a function of I_D
  - R_D will give us the drain current and R_S will shift the DC centre value
  - At the boundary between cutoff and saturation, both equation will apply; we need to get V_{DS} from these equations
  - If $I_D = 0$, then $V_D = V_{DD}$ since no current flows through the resistor, and $V_S = -V_{SS}$; this can give us a value for V_{DS}
  - At the boundary of triode, $V_{DS} = V_{GS} - V_T$
  - $V_{DS} = 0.6V_{GS} + 14.6$
  - We can get a final condition by using the saturation mode equations
  - This gives us V_{GS} and V_{DS} and lets us find R_S and V_D
  - Doing this however gets us very skewed limits – we're very close to cutoff‘

Lecture 19, Nov 22, 2023

Small Signal Models

- To model our amplifiers, we need 3 quantities: the voltage gain A_V, the input resistance/impedance R_{IN} and the output resistance/impedance R_{OUT}; to get these quantities, we need a model of small signals
  - We will mix DC and AC signals, assuming that the AC component is small
- Notation: All DC signals are represented with capital letter subscripts
  - $V_{IN} + v_{in} \to V_{OUT} + v_{out} = V_{OUT} + A_V v_{in}$
  - V_{OUT} is a function of V_{IN} only and v_{out} is a function of v_{in}
  - Note that often we will drop the DC parts, so that we have $v_{in} \to v_{out} = A_V v_{in}$, where A_V is the voltage gain
- The amplifier quantities A_V, R_{IN}, R_{OUT} are all functions of the DC bias point, but we assume that the DC bias point is fixed
  - This means we can solve for the 3 quantities first, and use any leftover adjustments to account for other quantities; note that often these quantities will already be overconstrained
- We can thus eliminate any DC components in the circuit and consider the time-varying components only; e.g. we can eliminate DC voltage sources (including at V_{DD} and V_{SS})
- However the MOSFET model is nonlinear, so we must Taylor expand it and use an approximation
  - $i_D = \frac{1}{2} k_n' \frac{W}{L} \left((V_{GS} + v_{gs}) - V_T\right)^2$
  - Expanding this, we will get a DC component plus $k_n' \frac{W}{L}(V_{GS} - V_T) v_{gs}$
  - $g_m = k_n' \frac{W}{L}(V_{GS} - V_T)$ is the *MOSFET transconductance parameter*, so $i_d = g_m v_{gs}$
  - Generally we will have some target, which we can use to solve for g_m and other parameters, and finally find the DC bias point using these parameters; we can also make other adjustments if we have more variables to work with
- Now we can replace the MOSFET with an equivalent default model, once we have the transconductance parameter
  - The model on the left accounts for the small signal itself and is the simplest possible model
  - The model on the right also accounts for channel-length modulation
    - This is a constant small signal current that always flows regardless of the applied voltage
    - This portion of the current isn't proportional to v_{gs}; this comes from the inaccuracies in our model
  - The resistance can be found as $r_o = \frac{|V_A|}{I_D}$; for drain currents in the milliamp range, this is often in the range of 10 to 100 $\text{k}\Omega$

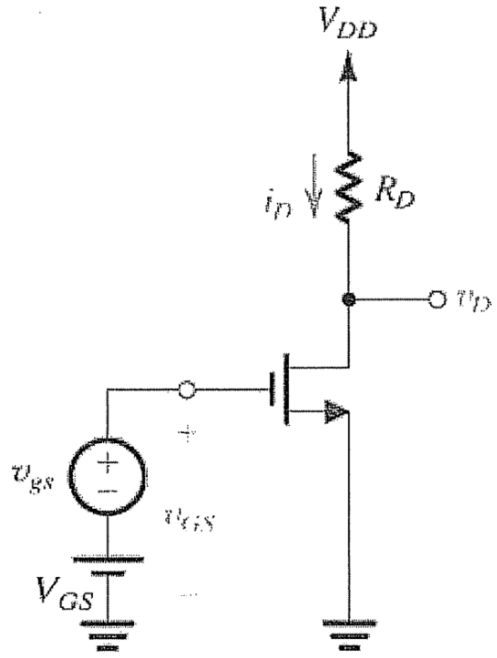

Figure 58: Amplifier circuit.

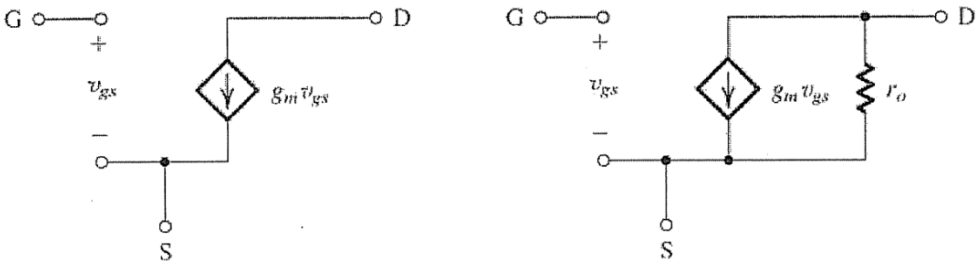

Figure 59: NMOS default model.

    * I_D is the DC drain current; V_A is a process parameter and is usually given (related to the MOSFET material properties)
  - The model on the right is more accurate, however we will often avoid using it, because usually it makes the analysis much more complicated without having too much effect

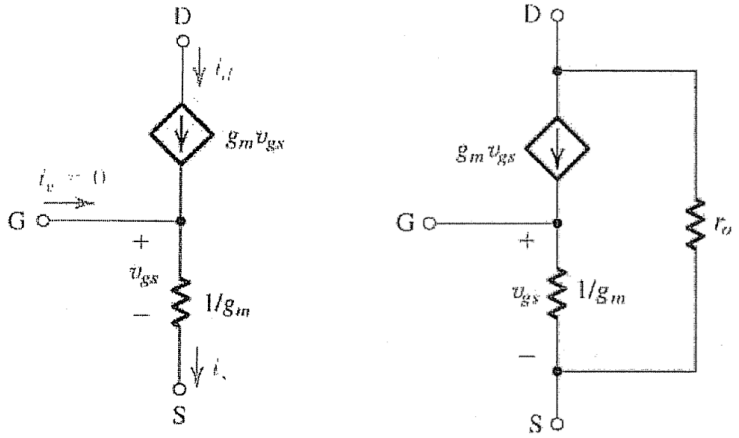

Figure 60: T-model of the MOSFET.

- Using circuit transformations, we can get several equivalent models; the one shown above is the T-model
  - This model is often much easier for calculating input and output resistances, if we are looking into the source or drain
  - Note that even though there appears to be a path from gate to ground, there would still be no gate current, due to the current from the current source exactly equalling the current through the resistor
  - The diagram on the right also incorporates channel-length modulation, which usually makes the analysis much more complicated
- The following procedure can be used to remove the DC bias point and its associated effects, leaving us with only the small signal part
  1. Solve the circuit to determine the DC bias point/quiescent (Q) point and calculate g_m, r_o for all MOSFETS
     - This is often given in most problems
  2. Replace the MOSFET with one of the previous models
  3. Replace all capacitors with a short, open, or constant impedance
     - This is because we usually assume an input of fixed frequency, so capacitors have constant impedances
     - Based on the relative size of the capacitor, we can decide which one to replace by; if the capacitor is sufficiently large, then it looks like a short circuit in AC; otherwise it may look like an open circuit or constant impedance
       * Usually coupling and bypass capacitors will be replaced by a short
       * There are some capacitances we don't have control of, e.g. the MOSFET parasitic capacitance; in this case we use an open circuit or constant impedance
     - In an exam scenario, it will normally be a short circuit
  4. Replace all DC constant voltage sources with short circuits (so that it effectively has a DC voltage of 0)
     - This means wherever we have a DC supply voltage, we will get a ground connection – this includes V_{SS} and V_{DD}
     - The only source of excitation is usually the MOSFET model itself
  5. Replace all DC constant current sources with open circuits (so that it effectively has a DC current of 0)
  6. Solve the resultant circuit to determine the gain, resistances, etc

Lecture 20, Nov 24, 2023

Example: Common Source Amplifier

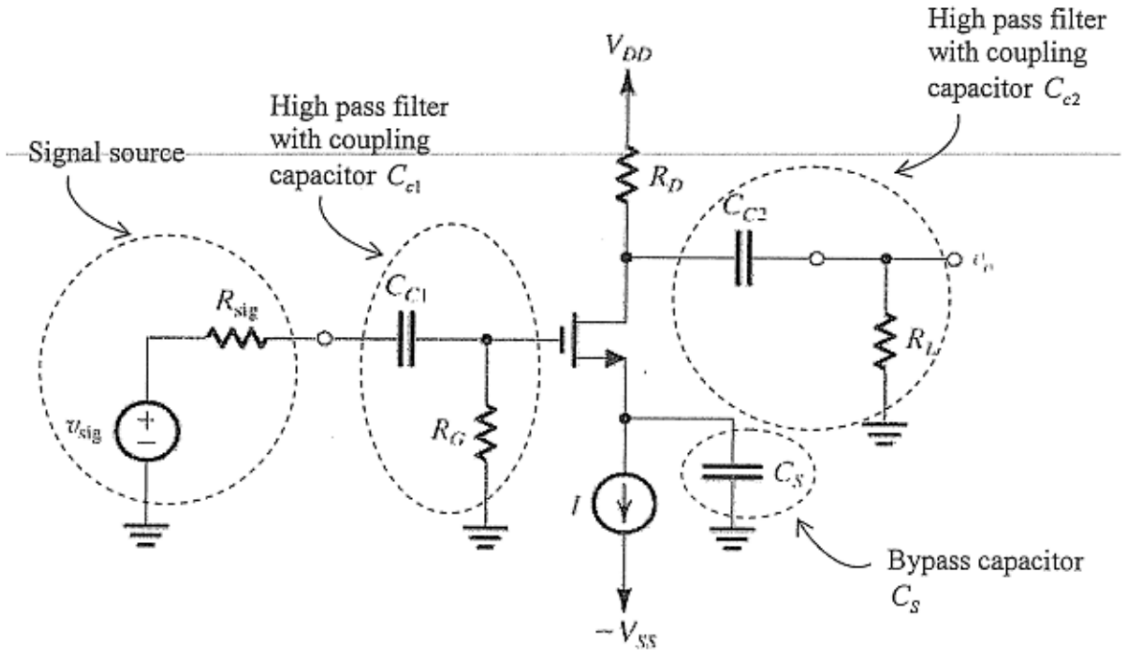

Figure 61: Example: Common source amplifier.

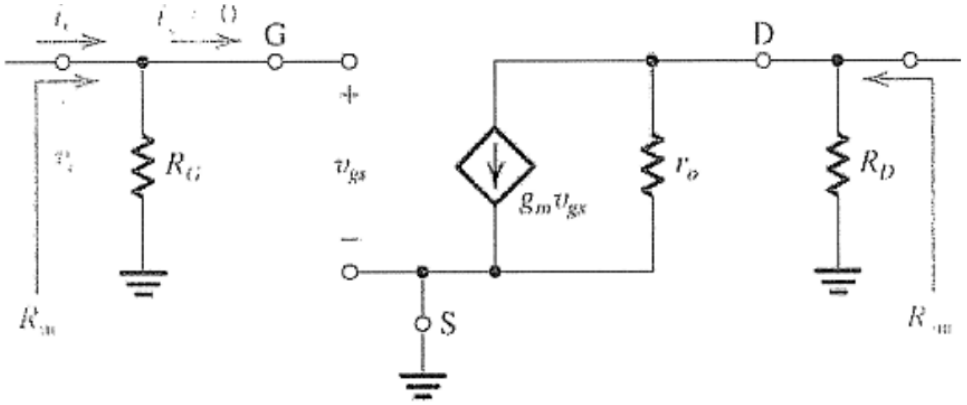

Figure 62: Transformed circuit of the example.

- Example: find the open circuit voltage gain, input resistance, and output resistance of the amplifier above
  - First transform the circuit:
    * Replace coupling capacitors$ C_{C1}, C_{C2} and bypass capacitor C_S with short circuits
    * Everything in the first circle is the driving input source; this is what gives us the time-varying signal, which gets driven through some finite output impedance
      - This is not a part of our amplifier, so quantities here should not appear in our solution
      - We define v_{in} at the node right after this, between R_{sig} and C_{C1}
    * The circle at the top right is the load, so like the input source, we also don't consider it as a part of our amplifier

    * Short circuit the voltage source at V_{DD} and replace the current source with an open circuit
      - Notice that if we didn't have the bypass capacitor, the circuit would not work, because after removing the current source the source would be floating
    * Replace the MOSFET with the default model
  - We will start by calculating the open-circuit voltage gain; for this we assume no loading effects whatsoever
    * Later on we will account for loading effects externally, so for now we won't consider it
    * Start by writing a node equation at v_{out} (the drain): $\frac{v_{out}}{R_D} + \frac{v_{out}}{r_0} + g_m v_{gs} = 0$
      - Note since we're calculating open loop gain, there's no current flowing in or out of the output
    * $v_{gs} = v_g - v_s = v_{in} - 0 = v_{in}$ so we have $\frac{v_{out}}{R_D} + \frac{v_{out}}{r_0} + g_m v_{in} = 0$ which we can now use to solve for $A_{v_0} = \frac{v_{out}}{v_{in}}$
    * This works out to $A_{v_0} = -g_m(r_0 \parallel R_D)$ or $-g_m R_D$ if ignoring channel length modulation
    * Note that since g_m and R_D are always positive, this is an inverting amplifier
  - Generally, common source amplifiers have high open-loop gain (more amplification) and high input resistance (loads input less), but generally high output resistance (susceptible to output loading)
    * These are often used near the input – the large gain bumps the signal up from the noise floor and the high input resistance is good
  - Now find the input resistance $R_{in} = \frac{v_{in}}{i_{in}}$
    * For this circuit, it is trivial: $R_{in} = R_G$ since no current goes through the gate
    * We can simply take a large R_G to increase the input resistance
      - R_G is part of the DC bias point but not any of the other variables, so we can more or less take it to be anything we want
  - The output resistance is $R_{out} = \frac{v_{out}}{i_{out}}$
    * Note we need to assume some value for v_{in} to do this calculation
    * We assume $v_{in} = 0$ to avoid double counting gain effects (i.e. we assume overall input voltage is constant)
    * If $v_{in} = 0, v_{gs} = 0$ so we get no current through the current source
    * Therefore the equivalent resistance is $r_0 \parallel R_D$ or R_D without CLM
  - Notice that we need a high R_D to get high open loop gain, but this raises the output resistance

Amplifier Equivalent Models

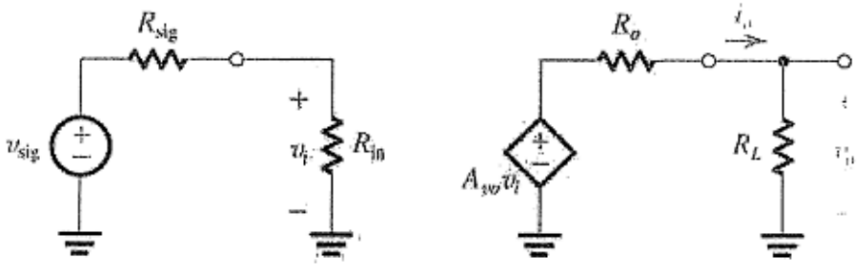

Figure 63: Equivalent model for the amplifier we solved above.

- The amplifier circuit we solved for above could be replaced by the equivalent model above, where the amplifier is in the middle; using this we can completely abstract away the amplifier
- The amplifier is replaced by R_{in} to ground, the voltage source $A_{v_0} v_{in}$ and output resistance R_{out}
  - Notice that R_{in} forms a voltage divider with R_{sig} and R_{out} with R_L
  - Both loading effects will reduce A_{v_0}; we only get this total gain with a zero R_{sig} and infinite R_L

- Otherwise the actual gain is $A_{v_{\text{total}}} = \left(\frac{R_{in}}{R_{in}+R_{sig}}\right) A_{v_0} \left(\frac{R_L}{R_L+R_{out}}\right)$

Example Amplifiers

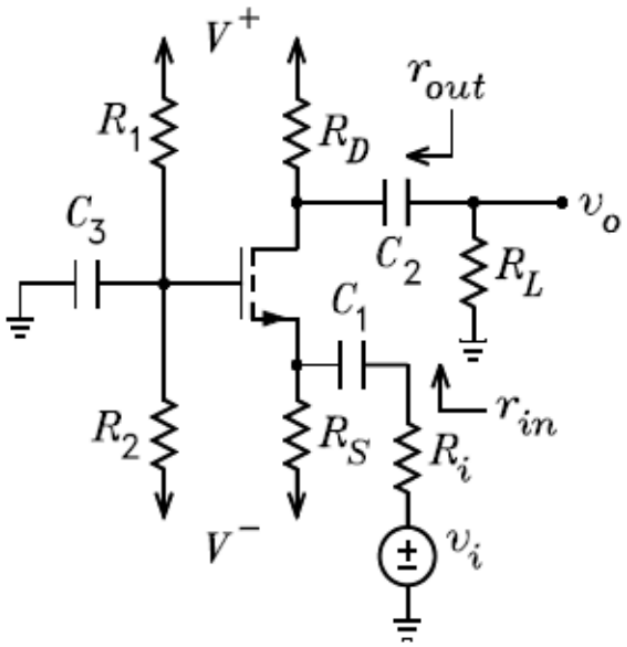

Figure 64: Example: Common gate amplifier.

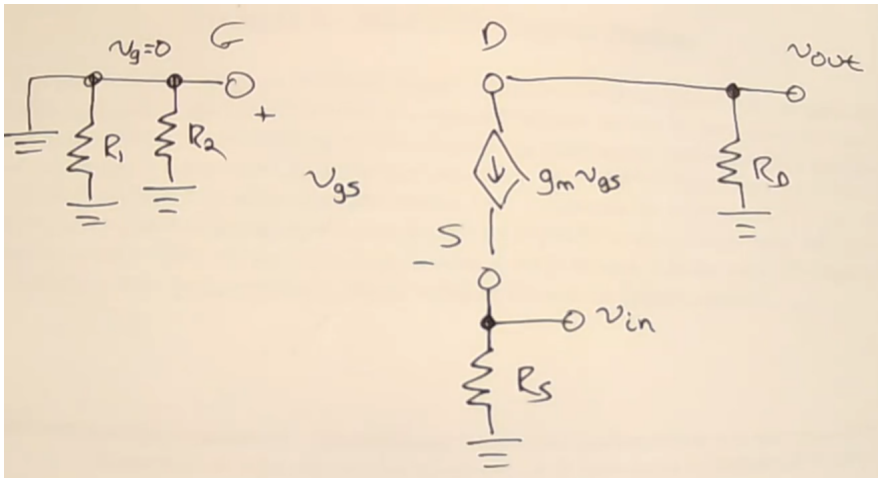

Figure 65: Transformed circuit.

- Example: Find the same 3 quantities in the circuit above, ignoring channel length modulation
  - First transform the circuit
    - R_L is part of the load and R_i is part of the source, so both can be removed
    - Replace C_1, C_2, C_3 with short circuits, V^+ and V^- to ground
    - Replace the MOSFET with the default model
  - Note that after shorting the capacitors, $v_g = 0$ so we can effectively ignore R_1, R_2
  - For A_{v_0} we can write a node equation at v_{out}: $\frac{v_{out}}{R_D} + g_m v_{gs} = 0$

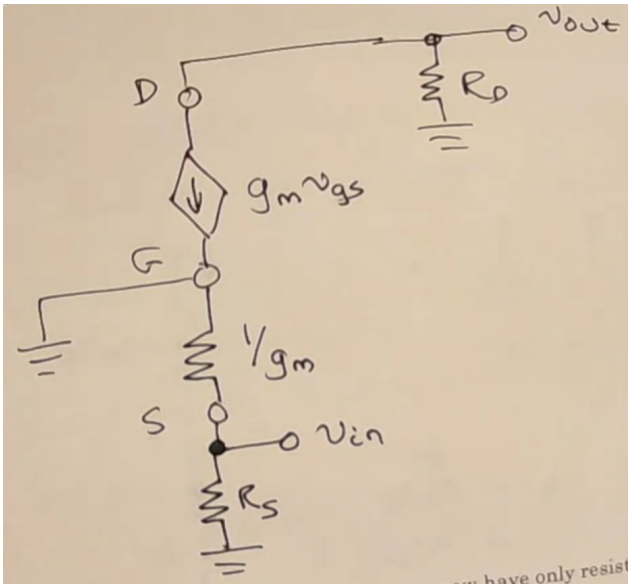

Figure 66: Transformed circuit using the T-model.

    * $v_{gs} = v_g - v_s = 0 - v_{in}$
    * Therefore $\frac{v_{out}}{R_D} - g_m v_{in} = 0$
    * $A_{v_0} = g_m R_D$
  - Notice that the open-loop gain is positive, so this is a non-inverting amplifier
  - Furthermore we can tweak g_m and R_D to potentially get a large open-loop gain
  - R_{in} and R_{out} are more complicated to solve due to the current source; we can redraw the circuit with the T-model to simplify things
  - With the T-model, we can easily tell that $R_{in} = R_S \parallel \frac{1}{gm}$
  - For R_{out}, with a $v_{in} = 0$ we have no current through the current source, so $R_{out} = R_D$

- Example: similar to the common source amplifier we solved before, but using a current mirror and no bypass capacitor
  - Note that this is not a proper amplifier, since we do not have a bypass capacitor
  - Normally this would not be solvable if we replaced the current mirror with a current source, but real world CLM effects provide a path for current
  - Use the same procedure to transform this circuit:
    * Replace V_{DD}, V_{SS} with shorts to ground
    * Remove input source and load
  - Notice that v_{gs_1} is a function of v_{in}, but v_{gs_2} and v_{gs_3} are not
    * The sources of both of these MOSFETs are grounded, and there is no path from v_{in} to their gates
    * In this scenario, we can assume $v_{gs_2} = v_{gs_3} = 0$ to simplify the circuit
  - Now we can eliminate the current source from the second MOSFET, leaving us with only r_{0_2}, a large resistance to ground
  - This is equivalent to having a source resistor on the original MOSFET circuit
    * Source resistors usually act like localized negative feedback – they reduce gain but improve some other parameters, such as lowering output resistance
    * However, unlike a normal source resistor, the CLM resistor is both hard to control and way too big
  - Write node equations:
    * At v_{s_1} or v_{D_2}: $\frac{v_{s_1}}{r_{0_2}} + \frac{v_{s_1} - v_{out}}{r_{0_1}} - g_{m_1} v_{gs_1} = 0$

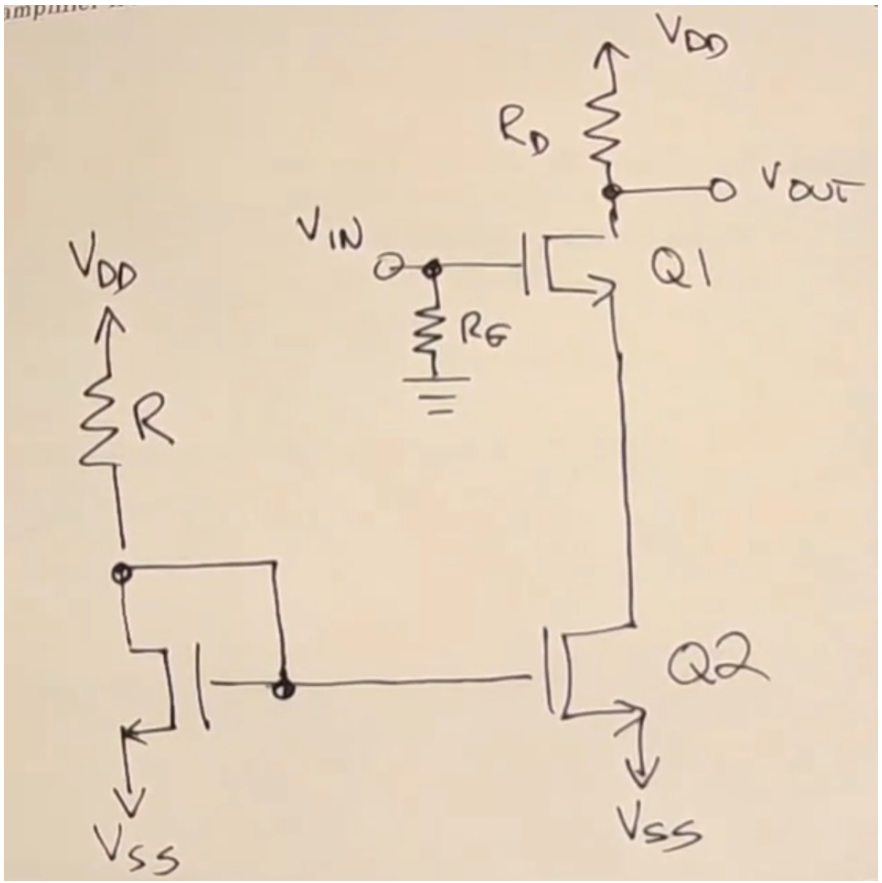

Figure 67: Second example circuit.

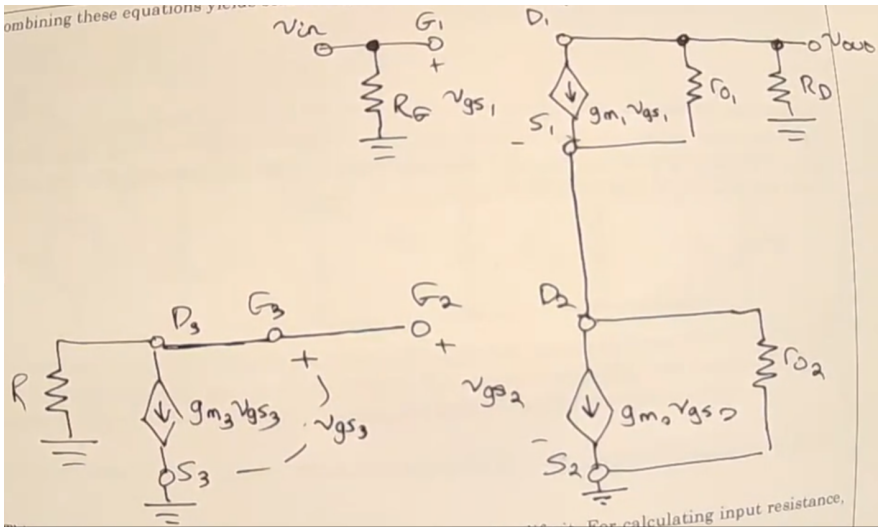

Figure 68: Transformed second example circuit.

- Note $v_{gs_1} = v_{in} - v_{s_1}$
  * At v_{out}: $\frac{v_{out}}{r_{0_1}} + \frac{v_{out} - v_{s_1}}{r_{0_1}} + g_{m_1} v_{gs_1} = 0$
  * Add the equations: $\frac{v_{s_1}}{r_{0_2}} + \frac{v_{out}}{r_{0_1}} = 0 \implies v_{s_1} = -\frac{r_{0_2}}{R_D} v_{out}$
  * Substitute into one of the equations, and $A_{v_0} = \frac{v_{out}}{v_{in}} = -\frac{g_{m_1} r_{0_1} R_D}{g_{m_1} r_{0_1} r_{0_2} + r_{0_1} + r_{0_2} + R_D}$
- Sine the CLM resistances are high, this is approximately $\frac{R_D}{r_{0_2}}$
  * As expected, the negative feedback reduces the gain, approximately by dividing by the resistance value
  * However since r_{0_2} is much bigger than R_D, we will have a gain much less than 1, so this is not practical
  * This is why source resistors are typically in the ohms or hundreds of ohms range
- Input resistance is simply R_G, which has not changed
- Recall that when calculating output resistance only, we assume an input voltage of zero to avoid double-counting gain effects
  * Assuming $v_{in} = 0$ gives us $v_{gs_1} = -v_{s_1}$, which is not necessarily zero
  * We can brute force this by using a test output current
  * However in this case we have a *cascode connection*, we can replace the entire thing with a single resistor to ground R_A
  * $R_A = (1 + g_{m_1} r_{0_1}) r_{0_2} + r_{0_1} \approx g_{m_1} r_{0_1} r_{0_2}$
  * Therefore the output resistance is simply $R_A \parallel R_D$, but since R_D is much smaller than R_A, the output resistance is still about R_D

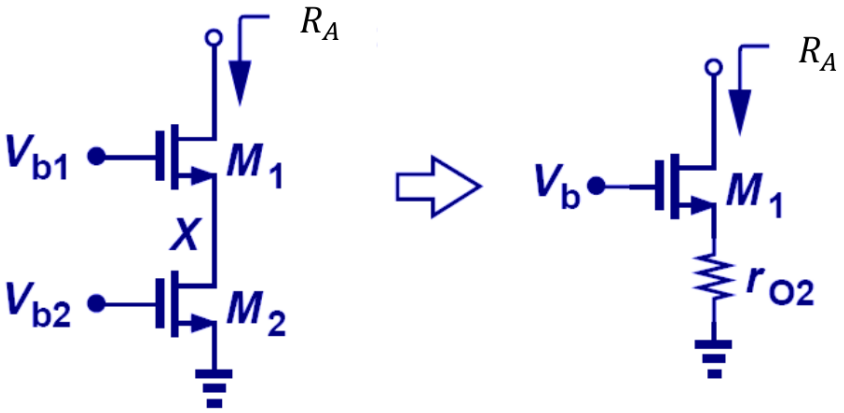

Figure 69: Cascode connection.

Lecture 21, Nov 29, 2023

Multi-Stage Amplifier Example

- Typically, for a multi-transistor amplifier, we can look at positions of the capacitors to draw dividing lines
  - Everything to the right of C_1 and the left of C_3 is the actual amplifier
  - C_2 divides the two individual amplifier stages
- Because we have a model for loading effects, we can analyze each stage separately
- The first stage is a common-gate amplifier, while the second stage is a common drain amplifier
- For a common-gate amplifier, as we have derived, $A_{v_{g_1}} = g_{m_1} R_{D_1}, R_{IN_1} = R_{S_1} \parallel \frac{1}{g_{m_1}}, R_{OUT_1} = R_{D_1}$
  - We can see that the standard results do not change if we draw this out in small signal domain

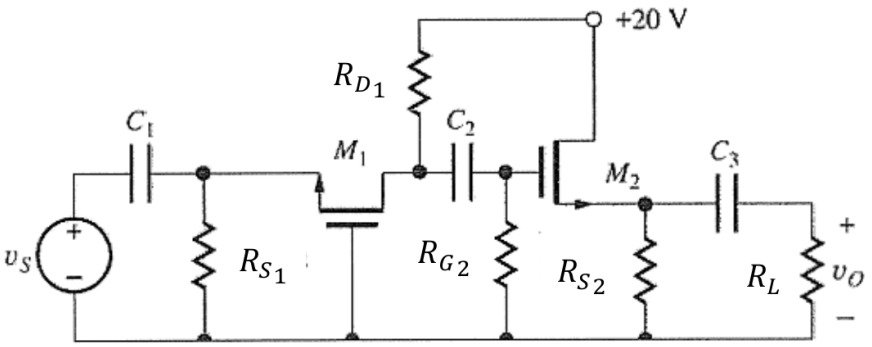

Figure 70: Multi-stage amplifier.

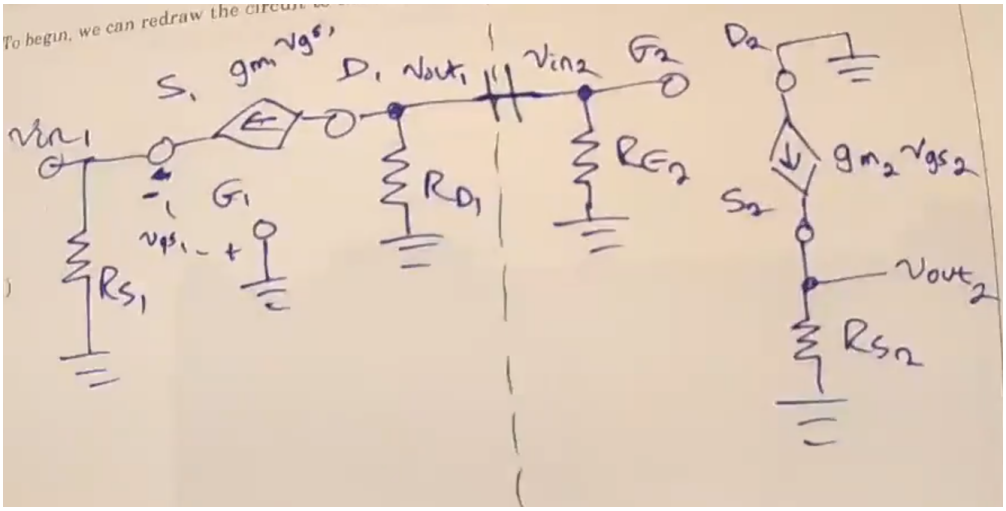

Figure 71: Amplifier in small signal domain.

- For the common-drain amplifier:
  - Redraw the circuit using a T-model
  - For R_{out}:
    * Assuming $v_{in} = 0$, the gate is grounded
    * $R_{out} = R_{S_2} \parallel \frac{1}{g_{m_2}}$
    * Source resistors tend to be small (kilohms or smaller), but $\frac{1}{g_m}$ is usually in the range of ohms to tens of ohms, so the second term will dominate
    * This gives us an output resistance in the range of tens of ohms or smaller, which is good
  - For R_{in}, we simply have R_{G_2}, since no current flows into the gate
    * We can easily make R_{in} relatively large
  - For A_{v_0}:
    * We can write a node equation at v_{out_2}
    * $\frac{v_{out_2}}{R_{S_2}} - g_{m_2} v_{gs_2} = 0$ where $v_{gs_2} = v_{in_2} - v_{out_2}$
    * $A_{v_0} = \frac{g_{m_2} R_{S_2}}{g_{m_2} R_{S_2} + 1}$
    * Note since typically $g_{m_2} R_{S_2} \gg 1$, the gain is close to unity; in fact, the gain cannot ever be greater than 1
  - This configuration is often called a source-follower – typically, it follows the voltage at the source without amplification, but increases the available power that can be output
- The common-gate amplifier amplifies the voltage, while the common-drain amplifier amplifies the power
- Now we can solve for the input/output resistances and voltage gain for the whole circuit
  - R_{in} for the whole circuit is simply R_{in_1}
  - R_{out} for the whole circuit is simply R_{out_2}, assuming an input voltage of zero
  - We don't have information about the source and load, so we will find the open circuit gain A_{v_0} for the whole circuit
  - $A_{v_0} = A_{v_{0_1}} A_{v_{0_2}} \frac{R_{in_2}}{R_{in_2} + R_{out_1}}$
  - In general, for multiple stages, the overall input resistance is the input resistance of the first stage; the overall output resistance is the output resistance of the last stage; the voltage gain is the product of all voltage gains, with a resistor divider between each pair of stages

Lecture 22, Dec 1, 2023